PRELIMINARY BEAM TEST RESULTS OF THE TLS LONGITUDINAL DAMPER WITH HIGH PERFORMANCE DSP MODULES

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Abstract

A bunch-by-bunch longitudinal feedback system that based on the state-of-the-art technology in the DSP industry is being developed for the Taiwan Light Source (TLS). Special design of the fast digital electronics provides the flexibility of using high performance VME DSP modules that are recently commercially available. Each of these modules has four 200 MHz fixed point processors with a highly parallel and deterministic architecture in CPU core design. With an aggregate progressing speed up to several thousands MIPS per board, total number of DSP chips required is significantly reduced. Testing of the system on the TLS storage ring is in progress. Preliminary beam test results on longitudinal coupled-bunch oscillation observations and feedback are reported.

1 INTRODUCTION

The goal of this study is to develop a DSP-based bunch-by-bunch longitudinal feedback system to stabilize phase oscillations of each of the two hundred bunches in the 1.5 GeV TLS storage ring that operates at a bunch crossing frequency of 500 MHz [1,2]. In our storage ring upgrade plan, a Cornell-type single cell super-conducting RF system will be installed because of its lower higher-order-mode contains as well as its higher achievable accelerating voltage that is beneficial to beam lifetime improvement. Operating beam current will be increased from the existing value of 200 mA to 500 mA. Under such high intensity operating condition, an efficient longitudinal feedback system is still considered to be essential.

The original digital electronics design for this system employs commercially available DSP boards with the 60 MHz TMS320C44 processors and therefore 'C4x communication ports are used for data handshaking between the DSP modules and fast ADC/DEMUX or DAC/MUX circuit [3]. As a result of the relatively slow clock rate and conventional CPU architecture of these chips, few tens of processors has to be used for a typical longitudinal feedback system that are designed for synchrotron radiation light sources or for high intensity particle factories for high energy physics [4]. Thanks to the rapidly growing DSP technology, VME modules equipped with high speed fixed point processors that has more elaborate CPU architecture and running at even faster clock rate is now commercially available. To take the advantages of their high performance for digital signal processing, it is reasonable enough to modify the original design to include them into the system. Fortunately, with the 'C4x compatible communication ports interface provided by the vendor of the DSP modules and the flexibility of the CPLD controller in the ADC/DEMUX and DAC/MUX circuits we developed in house for data handshaking, there are just only minor modifications for our purposes.

We reported in this article the changes we have been made on the previous design for using these DSP modules and some experiences in using them.

2 MODIFICATIONS IN FAST DIGITAL ELECTRONICS DESIGN

2.1 The DSP Modules

Two Pentek 4290 VME DSP modules that has four TI TMS320C6201 200 MHz fixed-point processors are employed in this newer version of system design. The announced aggregate peak processing speed for each DSP board is 6400 MIPS [5]. The 'C6201 processor has a highly parallel and deterministic architecture, called VelociTI, in its CPU core design. It performs eight 32-bit instructions in a single clock cycle of 5 nsec. However, the software development for 'C6x is quite different from conventional DSPs. For efficient operations, it requires special cares in algorithm development such that breaking the parallelism should be avoided. Various memory and I/O resources are designed for each of the four 'C6201 DSP chips. Each DSP chip takes care of the data processing for 25 bunches. Since there is an on-board 256kB dual port memory for each chip, the maximum record length of sampled data is 10 kB per bunch. Since the natural sampling frequency is 2.5 MHz and the down sampling ratio is chosen at 20, 10 kB corresponds to a record time of 80 msec for a sampling period of 8μsec for each bunch.

Global bus resources are accessible by all 'C6201and VMEbus. Data stored in 256kB dual port memories can be used for longitudinal bunch dynamics observations without interrupting the feedback system operation.

2.2 The 'C4x Compatible Communication Port Interface

Various types of mezzanine interface adapters for application-specific front panel I/O of the 4920 module such as 'C4x compatible communication ports, gigabit

serial links etc. are available. Since we use 'C4x communication ports in our previous design, the Pentek 6223 'C4x compatible communication port adapter VIM modules were used. There is a 2kx32 bits BI-FIFO connects data streaming devices located on 6223 to the V-bus which connected the nearby 'C6201. Data transfer rate can be as high as 400 MB/sec.

2.3 The Fast ADC/DEMUX and the DAC/MUX Units

The fast ADC has two 250 MHz ECL signal outputs that are 180° out of phase with each other. Each channel of the 250 MHz ECL output from ADC is then de-multiplexed into four channels by using the MC100E445 serial-to-parallel converter. Therefore, the data transfer rate is slowed down by a factor of four on each channel at the serial-to-parallel converter output. Data in ECL logic are then converted into TTL logic before they are stored in the FIFO memories. Down sampling and data transfer from FIFO memories to the 6223 VIM module are controlled by a CPLD implemented controller. It takes the advantage of in-system-programmability that the control logic may change from time to time during system integration and commissioning.

The multiplexer in the DAC/MUX unit receives data from eight DSP chips in the DSP modules (via communication ports on 6223) that represent filtered phase errors. It reorganizes these data in proper sequence and repeat its output for 20 turns. And these data are converted back to analog signal by a fast DAC (figure 1) and are send to the to the modulator for kick voltage amplitude modulation.

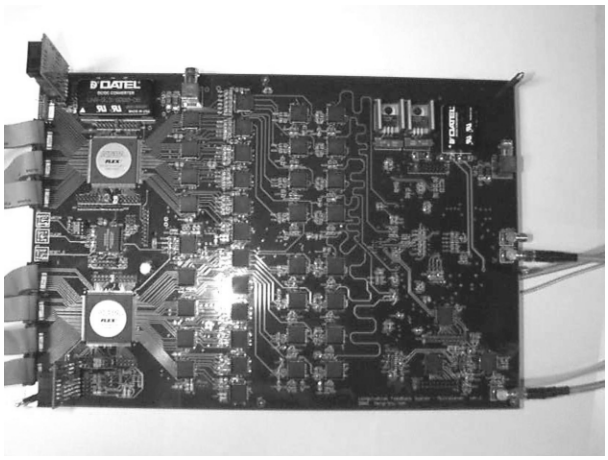

Figure 1: The DAC/MUX unit developed for the TLS longitudinal damper

The ADC/DEMUX, DAC/MUX and DSP modules has been integrated and tested with an artificial analog waveform is applied to the ADC/DEMUX input. The data representing the digitized signal by the ADC/DEMUX are transferred to the DSP modules and have been stored in the local memory near each DSP chips. These data are accessed by the host computer on the VME crate via global bus and are displaced (figure 2). The waveform in figure 2 is identical to the input analog waveform.

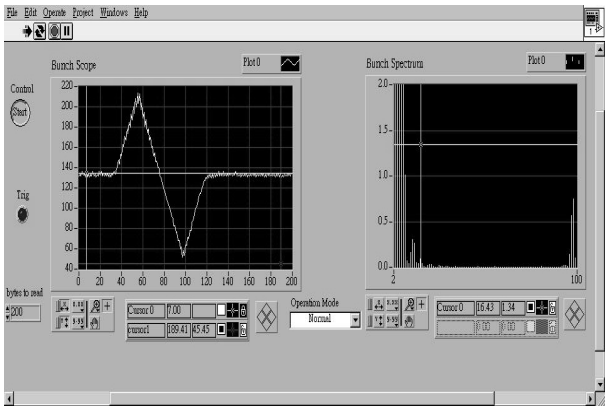

Figure 2: A display of data of the digitized signal transferred to the DSP chips.

These data are also send to the DAC/MUX from the DSPs. Figure 3 shows the analog signal output from the DAC/MUX board measured by digital oscilloscope. Good agreement between these signals is obvious.

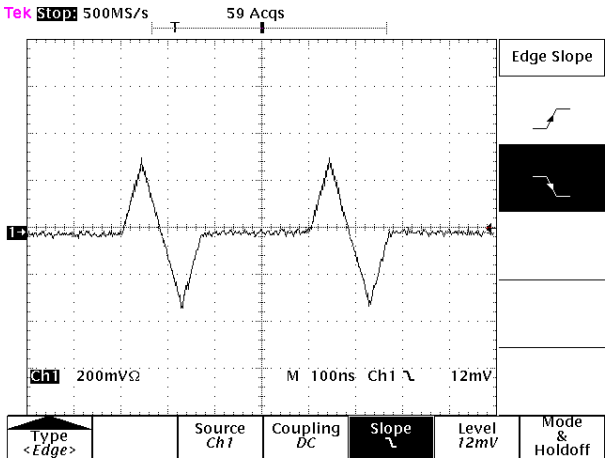

Figure 3: Reconstructed artificial signal by the DAC/MUX board.

3 OBSERVATION OF LONGITUDINAL COUPLED-BUNCH OSCILLATIONS

Bunch phase oscillations of 200 bunches can be recorded by using the feedback system electronics. Bunch phase errors for a stored beam of approximately 120 mA has been recorded for 8 msec (1024 samples). Since appropriate off-line data analysis tools are not available at the time this article is prepared, only phase oscillations of five neighboring bunches are depicted in figure 4. The vertical axis is the bunch phase errors in arbitrary unit and the oscillation centers (i.e. the bunch synchronous phases) are chosen arbitrary for clarity.

All bunches are oscillating at synchrotron frequency that agrees with the theoretical prediction. As shown in this figure, the bunch phase oscillations has an amplitude modulation at low frequencies.

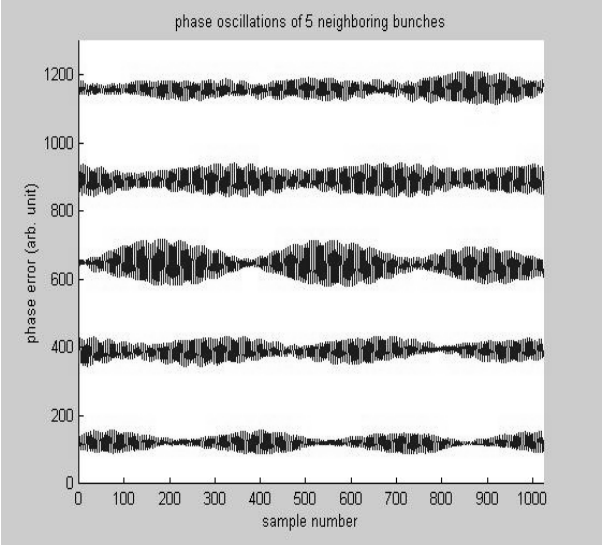

Figure 4: Raw data representing the phase oscillations of five neighboring bunches.

4 FEEDBACK RESULTS

Some preliminary feedback experiments have been carried out at low beam current. As shown in the spectrum of signal picked up by stripline (figure 5) from a 30 mA beam, side-bands in the middle part of the spectrum is mainly contributed by longitudinal coupled-bunch instability. Revolution harmonics near rf frequency at 500 MHz and also the harmonics of rf frequency are a result of the non-uniform beam filling pattern.

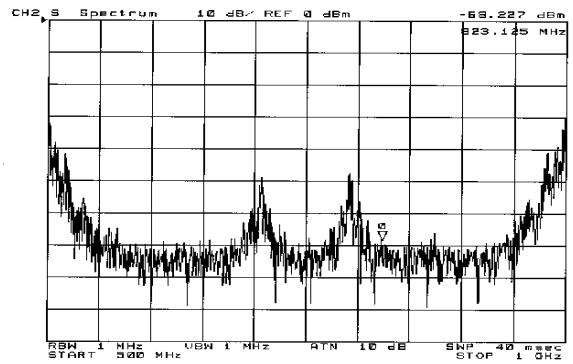

Figure 5: Beam spectrum at 30 mA with longitudinal feedback turned off

As a first trial, the bunch phase errors are directly applied to the modulator such that the kicker voltage is amplitude modulated. With the feedback system turned on, phase of the kick voltage and synchronization between signals are adjusted, anti-damping of bunch phase oscillations has been observed. However, amplitudes of side-bands in the middle part of the spectrum are clearly reduced as we multiply the bunch phase errors were multiplied by a negative sign (figure 6).

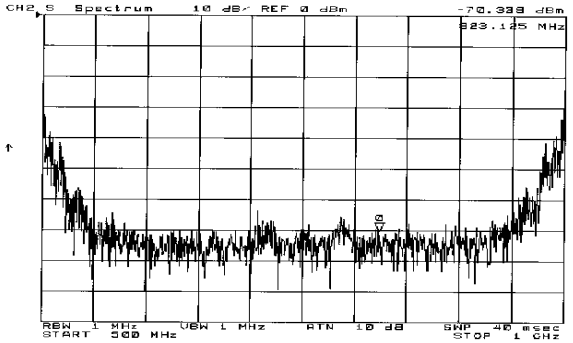

Figure 6: Beam spectrum at 30 mA with longitudinal feedback turned on.

5 DISCUSSION

We have successfully built the circuits for digital signal processing electronics such that high performance DSP modules can be used. Environment for observation of longitudinal coupled-bunch oscillations has been developed. Raw data record of bunch phase oscillations for 80 msec can be obtained from the onboard local memories near each 'C6201 DSP chips via the global bus. Experiments on longitudinal feedback have been carried out at low beam current, preliminary result showing bunch phase oscillations have been damped. Residual side-bands may due to the non-optimized digital filter design. A 4-taps FIR filter has been implemented into the DSP algorithm, the time required for 25 bunches calculation is about 1 μsec. Experiments with 4-tap filters are still in progress.

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