A TRANSVERSE FEEDBACK SYSTEM (TFS) FOR THE HEAVY ION SYNCHROTRON (SIS) AT THE GSI

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Abstract

The German Research Facility for Heavy Ion Research (GSI) intends to increase the beam current in the synchrotron by a factor of 100 which can leads to transversal and longitudinal beam instabilities. In order to damp the coherent transverse beam oscillations a transverse feedback system (TFS) is going to be implemented in the ring. Since the TFS should work with coasting beams and also as the accelerator is ramping up in energy, the required time delay for the electrical signal path varies enormous (from 600ns to 5μs). Furthermore, a time step resolution of 1ns is required to maintain high damping efficiency. Since more signal processing is required in the system the control part of the TFS consists of a digital signal processor system combined with some analog parts. Because of the high frequency range of the analog signal from pickup (20 kHz to 40 MHz) a parallel processing strategy is used for the digital system. In this paper the design and detailed information about the realization of the TFS will be presented.

1 PARAMETERS OF THE SYSTEM

In the following Table 1. one can find the basic parameters of the synchrotron in GSI.

Table 1: Specifications of the ring

Circumference of the SIS	216.7 m
Number of the bunches	1-4 (optional 6)
Bunching factor	0.3
Bunch length (FWHM)	30 ns - 420 ns
Revolution time	765 ns - 4.6 μs
Q-horizontal	Q_H = 4.1 - 4.4
Q-vertical	Q_V =3.1 - 3.4
β = v/c	0.156 – 0.95
Injection energy	11.5 MeV/u
Acceleration time	100 ms- 400 ms

1.1 Introduction

The major components of the coupling impedance in the SIS ring are the resistive wall impedance and kicker impedance. The theoretical prediction for the instabilities rise time is 15 ms for the kicker impedance and 120 ms for the resistive wall impedance. Because the acceleration time is bigger than the instabilities rise time it is important to stabilize the beam as the accelerator is ramping up in energy.

2 DESCRIPTION OF THE SYSTEM

The system consists of two pickups, variable delay, power amplifier and kicker. In the following it's described only the digital part of the system because that is the main part of the TFS and is in-house development.

The system need for correct operation four data ramps – revolution time, A and B coefficients and V amplification factor. The new value of the revolution time is processed every 1 μs that means the control system can change value of the delay every 1 μs and thereby to maintain such a synchronization between particle time of flight in synchrotron from pickup to kicker and electronic delay in our feedback. It is possible to set the revolution time with precision better than 200 ps. For this purpose the analog fine variable delay in the range 0.02÷20 ns will be used. The dynamic range of the system can be changed about 20 dB by means of V amplification factor. A and B coefficients are multiplication coefficients for vector summation. During the acceleration the focusing art is changing from triplet to doublet and the focusing parameters of the ring (β, α, Q ..) are changing too. The betatron phase is changing as long as the tune in the ring is changing. With two selected beam position monitors, 90° degree betatron phase relation between the pickups electrode and the feedback kicker can be controlled by adjusting A and B coefficients. From this reason A and B coefficients are precalculated and are stored in the tables and they are used on line for setting up of the attenuators when the feedback system is running. The system can provide 16 different types of cycles. Each cycle has several coefficients. The challenging problem is to be able to change the parameters of the feedback system when the system is running.

2.1 Main parameters

The main part of the system consists of digital signal processor with dual port memory and the PZ3320 (320 macrocell SRAM based CPLD). The system is clocked at 100 MHz. The PZ3320, which is used for the data transfer, control logic and summation of the two 12 bit signals from ADC, was simulated by means of the XPLA software. Output 13 bits signal is after the processing converted back to the analog signal. The digital system is capable to process the analog signal in the frequency range from DC to 50 MHz. Dynamic range of the digital system is 67 dB. Advantage of the system is that during of

the acceleration process it is possible to set the delay time in the system with step 1 ns. This step value is important for the efficiency of the entire TFS.

The specifications for the design of the system are enumerated below. At power up the dual port memory addresses are initialized and the memory contents is filled with zero. The left side address– input – is set up with value corresponding to the value of the delay. The right side address– output – is filled with zero.

1. 12 bit system
2. frequency range for clocks is 40-100MHz
3. controls are for delay, initialization, coefficients and gain

In the Table 2. are shown some parameters for the TFS system.

Table 2: Specifications for the TFS

Min. delay (β=1)	630 ns (60ns)
Max. delay (β=0.16)	4800 ns (402ns)
Min. step	~ 1 ns
Frequency range of the analog signal	20 kHz – 40 MHz
Impedance	50 Ω
Dynamic range	> 60 dB

2.2 Main board

The task of the main board is the variable digital delay. The digital system is initialized only one times with the address word what represent our delay by injection and then new value of the delay during acceleration process is setting up only by means of one digital signal.

The both analog input signals AIN1 and AIN2 from the front-end electronics are sampled by ADC at 100 MSPS with 12-bit resolution. After the digitalisation process the digitalized AIN1 is stored in the MEMORY small. The time the data are stored number of cycles in the memory represents small delay between both pickup (50ns ÷ 1μs). The both digitalised data are processed in the XCR3320 and then they are sent to the MEMORY big which represents the big delay between pickup electrode and feedback kicker. An adequate correction signal is constructed for feedback system.

2.3 Control board

The main task of the control board is processing of the data from the main control room (revolution time, A, B and V coefficients). For this purpose is used fixed point DSP TMS320C6201 clocked at 200 MHz (5ns instruction cycle). The VLIW (Very Long Instruction Word) architecture allows to execute up to eight instructions every cycle. The main DSP software is running in endless loop and is waiting for interrupt. Generating of the interrupt signal means that the new data are ready and DSP can read and process new data. For this purpose four independent interrupts are used. Since the interrupt signal is generated maximal every 1 μs (given by function generator), DSP has approximately 200 cycles for processing four interrupts. In this time DSP have to read data, process and calculate new data and after processing distribute the data to the main board.

2.4 Practical realisation

The transverse feedback processing electronics will be made of two VME chassis: one for the horizontal and one for the vertical plane. Each of them will host one main board, control board, two fine delays (between two pickups and pickup and kicker), four function generators (revolution time, A, B and V coefficients) and some I/O cards. The VME bus will be used to initialize, control and monitor the system. One of the technological challenges is to implement a high speed digital signal processing system at a peak data processing rate of 500 MBytes/s (300 Mbytes/s input, 175Mbytes/s output + 25Mbytes/s controlling). The both boards are in-house developments.

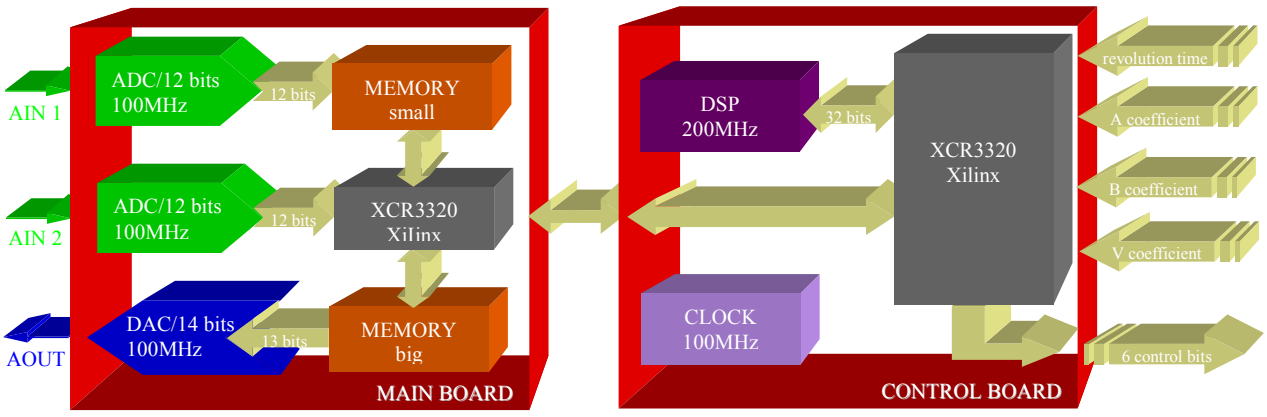

Figure 1: Principal scheme of the main and controlling board showing the main components.

2.5 Circuit board layout and fabrications

To keep the data signals in synchronous with each other, propagation delay have to be carefully controlled during circuit board layout. The work of PCB layout is complicated by the mixed signals running at high speed require impedance control, skew control and avoid cross talks between signals. There are the five signal layers and three power/ground layers so that the interface between layers can be avoided.

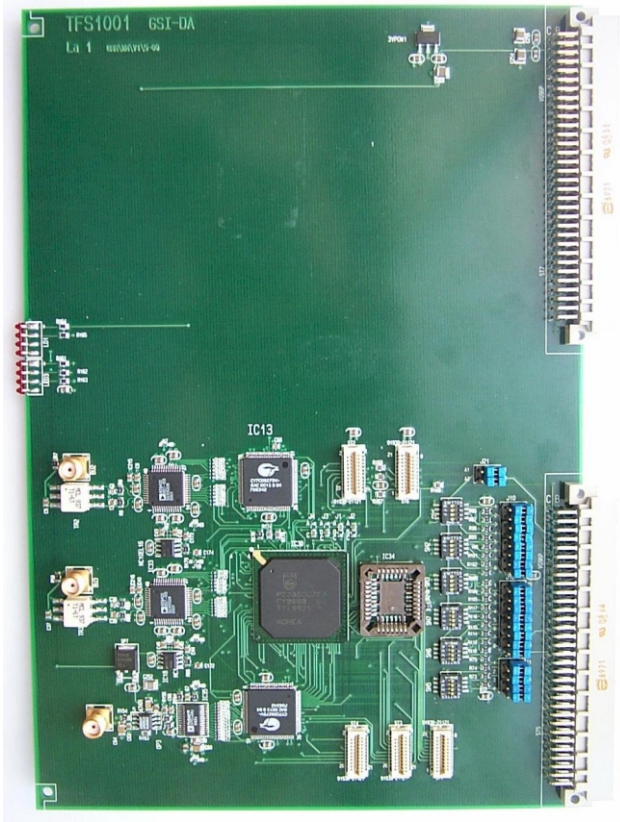

Figure 2: Full layout of the main board showing the all components.

2.6 Software environment

In order to develop, commission and operate TFS system efficiently, an integrated development environment running on PC is used. This software development system is a PC based JTAG emulator. The code composer is a system development tool that supports an integrated development environment for TMS320C6x. This environment is used not only for edit, compile and debug of the software but also for analyze signals graphically (including Eye Diagnostic, Constellation Diagnostic, FFT Waterfall).

3 DISCUSSIONS

Simulations carried out with the machine/feedback simulator show that the feedback performance degrades with betatron tune shift when the number of processing revolution periods increases. Therefore, the time during which the data remain in the main board must be minimized as well as any delay on every component of the feedback chain.

4 CONCLUSIONS

The TFS at the GSI is developed and is undergoing testing now. Overall bandwidth of the system is 20 kHz to 40 MHz. Four 200 Watt power amplifiers are used to drive the feedback kicker providing 55 dB total system gain.

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