INTERLOCK – THE MACHINE PROTECTION FUNCTION OF LIBERA BRILLIANCE

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Abstract

An interlock block for a Beam Position Monitor (BPM) has been developed. Customer requirements have been built-in and concurrent testing took place already in the development phase. The interlock can be switched on and off and operation in gain dependent mode can be selected. The later determines at what input signal level the interlock starts operation. Position data at 10 ksps is used to detect if the the beam is outside predefined limits, separate for X and Y directions. Moderate filtering is performed on both X and Y position data to avoid glitches. To avoid situations where a BPM reports illegal position data due to analog to digital converter (ADC) saturation an additional circuit for ADC peak detection has been developed. Interlock detection with accompanying circuitry has been realized entirely within the FPGA. Interlock output operates as a monostable circuit. Current implementation fulfils the requirement of detecting an invalid beam position within 10 ms. Interlock settings can be remotely set over the network.

INTRODUCTION

The interlock subsystem on each Beam Position Monitor (BPM) device is a part of the larger accelerator (machine) protection system. Its main task is to prevent modes of machine operation that can harm accelerator systems as a result of beam deviations away from normal set points. The task of each BPM is to properly measure the position of the beam and to activate interlock output if the beam is outside predefined limits. This output signal is fed to the interlock signal concentrator, where a decision logic is located. Depending on the BPM position in accelerator ring and overall machine protection strategy the system decides when the beam needs to be dumped. To prevent false alarms more than one BPM may be selected to report interlock interrupts, however, a more sophisticated logic is required to implement this mechanism. A basic requirement was set for an invalid beam position to be detected in less than 10 ms time.

IMPLEMENTATION

Following the basic requirement that any invalid position needs to trigger the interlock a basic block diagram of the position detection circuit is presented in the figure below.

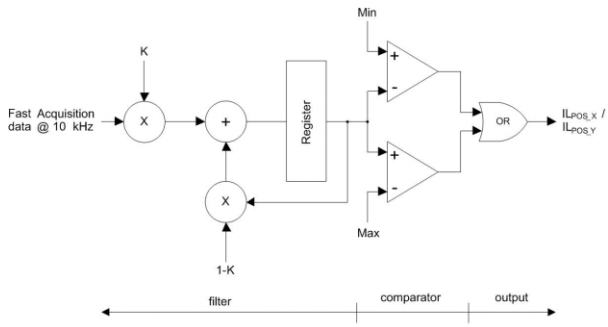

Figure 1: Position comparator implementation

At the input a simple IIR filter has been added to allow users to filter out possible spikes in the reported BPM position. A simple filter topology was selected as it can be very easily implemented within the FPGA. BPM position data is available at several data rates. As a compromise between the response time and measurement noise the selected data rate is 10 kHz filtered and has a bandwidth of approx 2kHz. At this rate the position noise is in the range of 1 μm. This value is a few orders of magnitude lower than than a typical interlock position limit of around 1 mm. At 10 kHz data rate around 100 samples of position data are available in the time required to activate the interlock. BPMs measure X and Y positions therefore two sets of position detection circuits are required. Both position inputs need to operate with the true position data, free of all inherent offsets, regardless of their origin.

Besides X and Y position limits the interlock circuit also requires several other inputs for configuration. First input is the on/off switch. No separate X and Y enable inputs are provided. To disable only one dimension of interlock the limits must be set to a value that can never be reached.

BPM users prefer switching the interlock off at lower beam currents as there is no need for protecting the machine. For this purpose a selection between the BPM gain dependent interlock and continuously operational interlock was added. With lower input signals at low currents higher front-end gain in the BPM is required. Instead of providing the beam current value from external or calculating the beam current from the input level and gain setting a simpler solution is used. We simply assume that the gain is always steady or increasing with lowering the current and that the gain is a monotonic function. Comparing gain setting with a predefined limit determines whether the interlock is operational or not. If there are multiple points within the BPM where the gain can be set, the simplest solution is to use the sum of gains (or attenuators) to be compared to the gain limit.

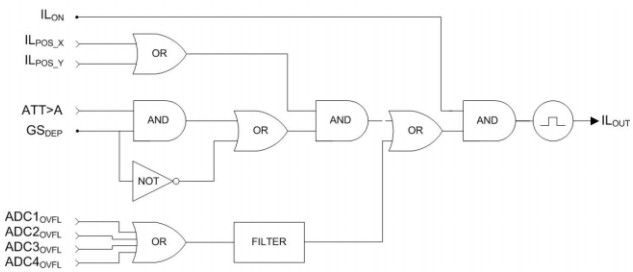

Figure 2: Interlock glue logic

As seen from the block diagram in figure 2 some glue logic is required to implement what has been described so far. There is one more input branch to the interlock circuit. The above described principle of operation is functional only in the case that position data is valid. This may not be true if any one of the BPM electrodes is saturated. Saturation can for instance be easily reached if automatic gain control is used but beam current changes cannot be followed. In the digital BPM if ADCs are saturated, the calculated position will be close to the centre. The beam position is calculated using the formula.

$$x = k * \frac{A - B - C + D}{A + B + C + D}$$

If the amplitudes from the four pickup electrodes A, B, C and D are at their maximum values the calculated position is 0. The same applies for the y axis. If we observe electrode amplitude data at revolution rate, ADC overflow can't be detected. Majority of the frequency components that indicate overflow, are removed from the spectra within filtering and decimation blocks in the digital receiver.

To detect saturation, a peak detector circuit was developed. It uses ADC rate data. A simple diode-like peak detector could be designed but we decided to use quasi quadrature detector instead. The sum of squares of $\pi/2$ apart samples is a good enough approximation of the square of the amplitude. This approach is useful even in the case that ADC sampling is not precisely in quadrature. Typical input signal frequency is around 30 MHz and the sampling clock frequency around 115 MHz. Using moderate filtering the resulting ripple in the amplitude can be efficiently removed.

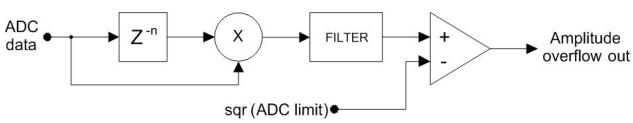

Figure 3: Quadrature detector and comparator implementation

Unfortunately the response time is inevitably sacrificed when filtering is applied. A Matlab script was used for calculating the filter coefficients. The main criteria for calculation is to achieve about the same amplitude ripple for all the accelerators.

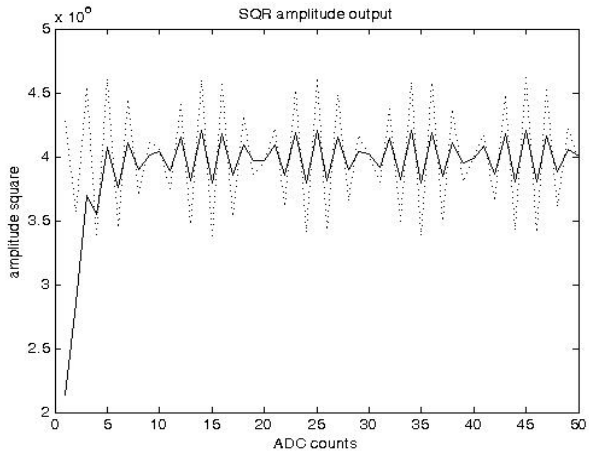

Figure 4: Filtered (solid line) and unfiltered signal (dotted line) from the amplitude detector

In order to reduce the required FPGA resources, a detection circuit is multiplexed between all four channels at the machine revolution rate. Such a solution can be used as the required reaction time is much longer than revolution period.

The interlock output is an optically decoupled switch (opto-coupler). It is important that the interlock circuitry does not trigger false alarms and that it reacts when required. For this purpose, an inactive interlock keeps the the switch closed. If a BPM fails for some reason, the interlock switch opens and thus triggers the interlock, reporting that the beam position protection mechanism is not operational.

The interlock output includes a monostable circuit that extends its active state for typically 10 ms beyond the time of valid interlock conditions. Interlock outputs are in some implementations connected to Programmable Logic Controllers. These are usually not fast enough to react to 1 ms or even shorter pulses but 10 ms pulses are long enough to be properly detected.

Interlock setting is performed through software, e.g. the BPM utility program. All parameters are passed as a command line parameters. Usually interlock setting is done during the BPM electronics startup, when the initialization script is executed. Good understanding of interlock operation is required due to a large number of parameters.

CONCLUSIONS

The interlock circuit presented here was developed based on requirements from the end-users. Already in the development phase there were many iterations that helped developers to implement the most convenient solution. Concurrent testing of the interlock implementation took place at customer sites. The current implementation has now been used for two years. Feedback from customers

indicate that the interlock is working properly. However due to many options in the interlock setting, significant support to the customers is required. The limitation that peak detector is working properly down to 5 % of the filling pattern is well known. The circuit could be improved using a peak searching algorithm that would be reset in a predefined period of time, expressed in integer number of machine turns.

REFERENCES

[1] Libera Brilliance & Electron - User Manual v1.82, Instrumentation Technologies, 2008

[2] Libera Electron Interlock - Quick Guide, Instrumentation Technologies, 2006