DIGITAL LLRF FOR ALBA STORAGE RING

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Abstract

ALBA is a 3 GeV, 400 mA, 3rd generation Synchrotron Light Source that is in the construction phase in Cerdanyola – Barcelona, Spain. The RF System will have to provide 3.6 MV of accelerating voltage and restore up to 540 kW of power to the electron beam. A Digital LLRF prototype has been developed for the Storage Ring RF Cavity. The prototype is based on the IQ modulation/demodulation technique and it has been implemented using a commercial cPCI FPGA board. The prototype has been installed in the high power RF lab of CELLS and tested to control up to 80 kW on the real Storage Ring Cavity. The test results of the control loops (amplitude, phase and tuning) will be presented, as well as the hardware structure (digital boards, analogue front ends, timing, etc.)

INTRODUCTION

The task of a LLRF system is to regulate the amplitude and phase of the RF field and the resonance frequency of the cavity to compensate for transient beam loading, ripples of the high voltage power supply and temperature variations.

The specifications of the ALBA RF and LLRF are summarized in Table 1.

Table 1: RF/LLRF specifications of the storage ring

Frequency	499.654	MHz
No. of cavities	6	
Cavity Shunt Impedance	3.3	MOhm
RF power (per cavity)	150	kW
RF voltage (per cavity)	600	kV
Beam current	400	mA
Beam power (per cavity)	90	kW
Amplitude stability	±0.1	%
Phase stability	±0.1	°
Bandwidth	> 15	kHz
Dynamic range	30	dB

The Digital LLRF (DLLRF) of ALBA is based on digital IQ modulation/demodulation technique carried out by a commercial cPCI FPGA board. The DLLRF is intended to control the amplitude and phase of the RF Cavity voltage within 0.1% and 0.1° respectively, as well as the resonance frequency of the cavity up to ±0.1º.

DLLRF HARDWARE

The main components of the DLLRF system are:

- Two analogue front ends for up/down conversion of the RF inputs
- Commercial cPCI boards with 16 ADCs, 8 DACs, two FPGA (Virtex-4) and two SDRAM (128Mbytes) from Lyrtech Ltd.
- An analogue and a digital timing system.

The conceptual design of the digital prototype is shown in Figure 1.

Analog Front Ends: Down and Upconversion

The analog front ends downconvert the RF signals (500MHz) to intermediate frequency (20MHz), by mixing the RF inputs with a 520MHz signal and by low pass filtering the output.

In overall 15 RF signals are downconverted. Two of them will be employed for the control loops (the cavity's voltage and the cavity's forward power voltage) and the other 13 RF signals, will be used for diagnostics of the RF plant (waveguides, circulator, load, IOT, etc)

The second task of the front end is to upconvert the control signals (DC) of the digital boards to 500MHz using an IQ modulator. Two drives are generated per plant (IOT1 drive and IOT2 drive) and thus, only 4 DACs out of the eight available are employed.

Timing Systems

The Digital Timing system provides a 80MHz clock for the FPGA boards, ADCs and DACs. This clock is generated in a board with a VCXO of 160MHz, locked with an external reference signal of 10MHz

The analog timing system provides the 520MHz signal required for the downconversion. This signal is obtained combining the Master Oscillator signal (500MHz) with a 20MHz signal. The combination is performed with an IQ modulator doing a single side band upconversion and filtering the output with a 520MHz helicoidal bandpass filter. The 20MHz signal is generated dividing the VCXO frequency (160MHz) by 8. This is done to ensure the IF signal outputs of the downconversion are perfectly synchronized with the 80MHz clock of the digital board.

Digital Boards

Two digital boards are used per each DLLRF system. One of them has 8 ADCs and 8DACs and will be used for the control loops (amplitude, phase and tuning). The other board has 8 ADCs and it will be used only for diagnostics purposes. Both boards have a Virtex-4, a 128Mbytes SDRAM, a Direct Memory Access Module (DMA), 32 Digital Inputs/Outputs and other communication ports.

DLLRF SOFTWARE

IQ Demodulation

The IF signals are sampled at 80MHz rate in the ADCs, a frequency four times higher than the IF. This provides an alternative sequence of the I and Q components (I, Q, -I, -Q…) as shown in Fig. 2.

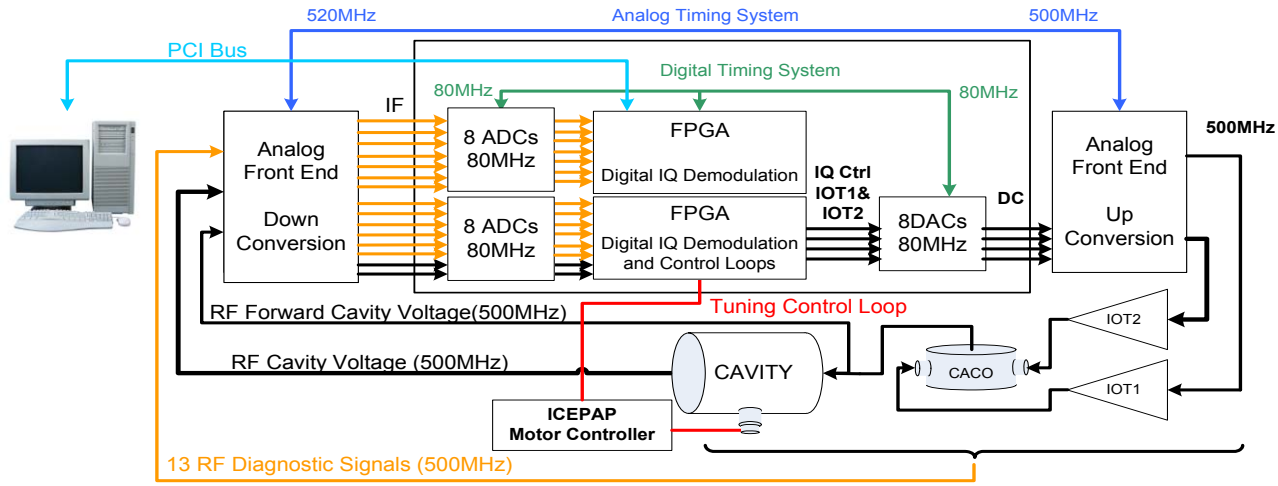


Figure 1: Digital LLRF Hardware Scheme.

This sequence is demultiplexed in two channels (I&Q). The sign of the I&Q signals determines in which phase quadrant we are working. (I&Q>0, first quadrant; I<0, Q>0, second quadrant, etc.) A software parameter of the FPGA allows choosing the quadrant of interest.

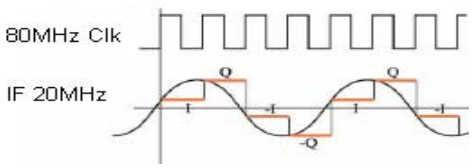


Figure 2: Digital IQ Demodulation.

Control Loops

The input of the amplitude and phase loops are the I&Q components of the cavity voltage signals. These components are sent to a software phase shifter to compensate any cable delay and afterwards, they are sent to two identical PI controllers. The proportional gain and the integral gain are parameters that can be adjusted through the GUI of the DLLRF. There is also an adjustable software limit which prevents the control output to reach too high values, avoiding any overload on the IOTs.

Another feature of the software allows disabling the loop and it permits working in open loop. This mode helps to study the step response of the system, the time delays of cables, components non linearities and so on.

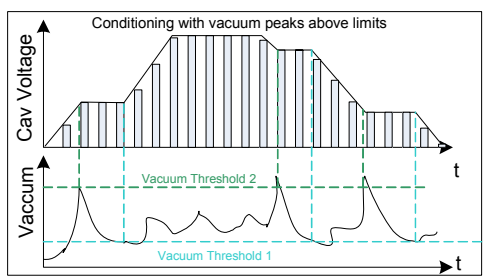
The tuning loop adjusts the resonance frequency moving a plunger in and out of the cavity body. To calculate the resonance point, the program calculates the phase difference between the cavity voltage and the cavity forward power voltage. The Cordic algorithm is employed to obtain this value. The digital I/O port of the digital board is used to send two digital signals to the Icepap or motor controller. One of these signals indicates the sense of the plunger movement (in or out) depending on the sign of the phase difference. The other signal indicates the number of steps that the plunger should be moved. A deadband with flexible limits has been implemented in order to avoid the plunger moving constantly in and out when it is closed to the resonance point.

The bandwidth of the tuning loop is limited by the plunger motor speed which cannot be moved faster than 2 kHz. Because of this, the I&Q inputs of the tuning loops are filtered employing a moving averaging, reducing the noise of the phase and achieving a resolution in phase better than 0.01°. With this slow filtering, the tuning loop is still fast enough to compensate the beam loading and any thermal drift that may change the resonance frequency point of the cavity.

Automatic Conditioning

An automatic conditioning mode has been implemented in the DLLRF. The amplitude of the cavity voltage is increased smoothly at a rate of 2mV per second (40mV corresponds to 0.65kW and 400mV corresponds to 80kW). Also the conditioning duty cycle is increased smoothly at a rate of 2% per second.

The equipment protection system of the RF plant (EPS) sends two digital signals to the DLLRF to indicate the vacuum level of the cavity. In case the vacuum is below a first threshold, the amplitude can be increased or decreased without any restriction, but in case the vacuum is above a second threshold the amplitude reference stops varying and it only continues the ramp when the vacuum is stabilized below the first vacuum threshold. This is done in order to minimise the vacuum trips and speed up the conditioning. A representative graph is shown in Figure 3.



Figrue 3: Automatic Conditioning.

Diagnostics and Communications

There are two systems to store the diagnostics signals of the loops (IQ errors, cavity voltage amplitude, cavity voltage phase, control signals, etc) and the diagnostic signals of the RF plant (IOT, CaCo, Circulator, Load). The first one is employed to study the long term stability and it acquires all these signals at a rate of 1 Hz (figure 6). The second one is a fast one meant to study transient responses, the noise of the signals and any fast variation effects. It sends decimated signals to the SDRAM at a rate of 80MHz. In case a failure occurs or a software trigger is activated, this data is retrieved and sent to the host PC for post mortem analysis (figure 5).

DLLRF TEST RESULTS

The DLLRF has been tested at the high power RF lab of ALBA. The stability of the amplitude, phase and tuning loop was measured as well as their bandwidth, figure 4.

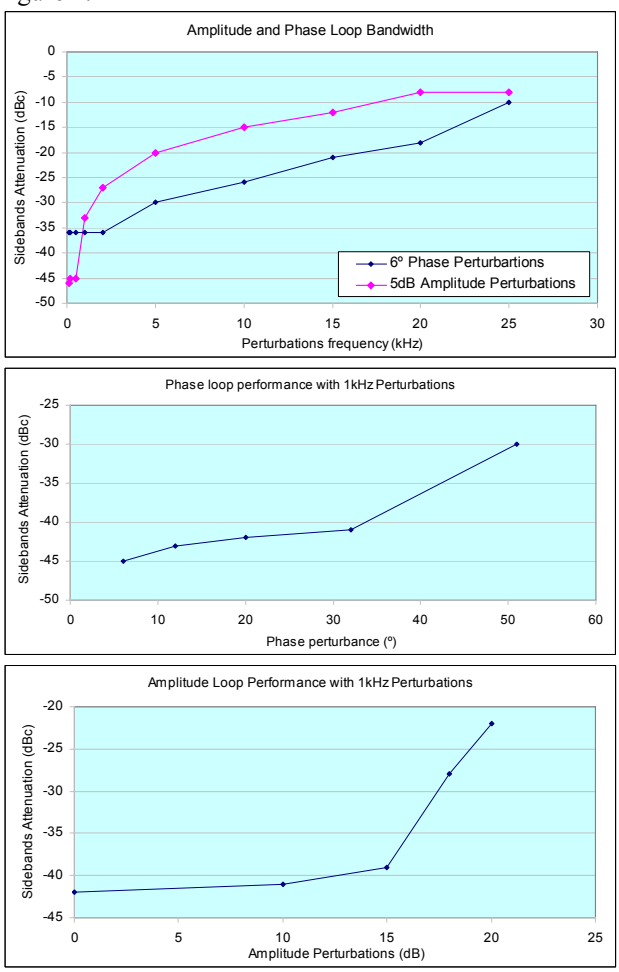


Figure 4: Bandwidth and ripples rejection of the loops.

The resolution of the PID loops was also measured at high power (75 kW) and the results are shown in Figure 5

The rms error of the amplitude loop is 0.11% at 80 MHz and 0.03% after filtering the I&Q cavity signals at 1 MHz rate. The rms error of the phase is 0.35º at 80 MHz and 0.1º at 1 MHz

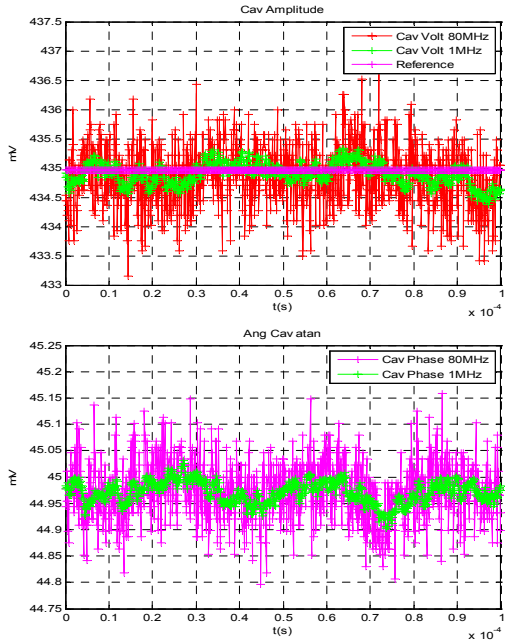


Figure 5: Loops resolution at high power (75kW).

Figure 6 shows how the tuning loop compensates a detuning of -10º after being switched on, bringing the phase to +1º. It also shows how the reflected power decreases from 1kW to some tens of W. After this, the thermal drift makes the cavity go out of tune in 30 seconds (phase going from +1º to +3º) and the reflected power increases up to 300W approximately. When this point is reached the plunger is moved again to -1º in less than 2 seconds.

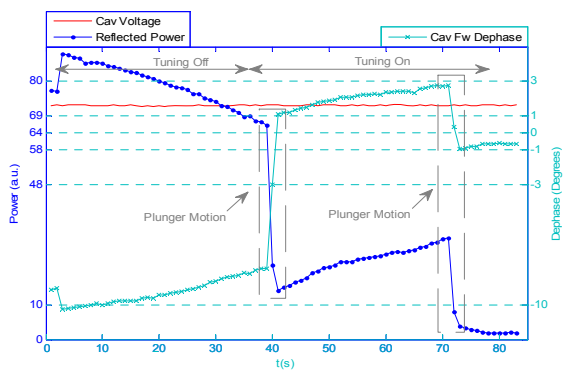


Figure 6: Tuning Loop

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