

AUTOMATIC SYSTEM FOR THE D.C. HIGH VOLTAGE QUALIFICATION OF THE SUPERCONDUCTING ELECTRICAL CIRCUITS OF THE LHC MACHINE

D. Bozzini, V. Chareyre, S. Russenschuck, CERN, Geneva, Switzerland
M. Bednarek, P. Jurkiewicz, A. Kotarba, J. Ludwin, S. Olek, HNINP, Krakow, Poland

Abstract

A d.c. high voltage test system has been developed to verify automatically the insulation resistance of the powering circuits of the LHC. In the most complex case, up to 72 circuits share the same volume inside cryogenic lines. Each circuit can have an insulation fault versus any other circuit or versus ground. The system is able to connect up to 80 circuits and apply a voltage up to 2 kV D.C. The leakage current flowing through each circuit is measured within a range of 1 nA to 1.6 mA. The matrix of measurements allows characterizing the paths taken by the currents and locating weak points of the insulation between circuits.

The system is composed of a D.C. voltage source and a data acquisition card. The card is able to measure with precision currents and voltages and to drive up to 5 high voltage switching modules offering 16 channels each. A LabVIEW application controls the system for an automatic and safe operation. This paper describes the hardware and software design, the testing methodology and the results obtained during the qualification of the LHC superconducting circuits.

INTRODUCTION

The LHC accelerator is composed of 1750 superconducting circuits [1]. Considering the large number of circuits and the limited volumes where the conductors are housed and routed, there is a considerable risk of electrical insulation faults. They may occur between circuits sharing the same superconducting cable segment, between conductors in different cables sharing the same cryo-line, and between circuit and ground. Electrical insulation faults are caused by damages during the assembly, by weak electrical insulation of elements composing the circuit, by thermo-mechanical contractions during the cryogenic cycles, or by the degradation of the insulating materials due to aging or cumulated radiation doses.

No commercial system was available on the market with the required sensitivity for the current leakage measurement and with the possibility to measure the current leakage flow path between tested circuits. Therefore the development, the prototyping phase and the series production of a d.c. high voltage qualification system has been done at CERN and it is presented in this paper. We refer to this system as the HVQ system in what follows.

SYSTEM REQUIREMENTS

Circuit parameters

The detailed electrical characteristics of all LHC circuits are available in [1]. The Nominal test parameters for the HVQ system are given in table 1. We distinguish the circuit for the main bending dipoles (MB), the focusing quadrupoles (MQ), the lattice sextupole correctors (MCS) and the dipole orbit correctors (MSCB). Parameters of primary importance for a high voltage qualification are the capacitance and the test voltage levels, while the other parameters are needed to adapt the construction of the system to the LHC working environment.

Table 1: Electrical characteristics of circuits.

Parameter	Unit	MB	MQ	MCS	MSCB
Magnet in series	-	154	47	154	1
Circuits	-	8	16	16	914
Inductance	H	15.7	0.268	$123 \cdot 10^{-3}$	2.84
Capacitance	F	$60 \cdot 10^{-6}$	$5.3 \cdot 10^{-6}$	$0.9 \cdot 10^{-6}$	$22 \cdot 10^{-9}$
Length	m	~2800	~2800	~2800	~5
Test voltage	V	1900	240	480	600

Operating modes

Two operating modes have been considered in accordance to the LHC requirements. The first allows the testing of each circuit, one after another, with a sequence composed of four phases: voltage ramp up, stabilization of the leakage current, measurement and voltage ramp down. In this mode, voltages up to 2 kV can be applied. For safety reason the system has to be always supervised by an operator. The second mode of operation is an online monitoring of leakage currents for periods longer than 3 weeks, i.e., for the cool down phase of a LHC sector. For this operating mode the maximum applicable voltage is limited to 50 V. The HVQ system can work autonomously and safely with a remote supervision.

Testing procedure

The testing procedure is first oriented on safety regulations to be applied when operating high voltage devices. As a basic rule, the system can only be switched on when all circuits to be measured are connected to the system. There is thus no need for test operator to intervene in the vicinity of live parts.

A typical test procedure unfolds in the following order: the HVQ system channels are connected to the terminals of all circuit to be tested; the connections to earth of all

tested circuits are then removed. The HVQ system is switched on and the control software is launched, executing the test sequence automatically. At the end of a successful test, the circuits are discharged internally and the system is switched off. The circuits are then manually connected to earth, which is a requirement for the disconnection of the system. This way of proceeding always grants the grounding of the circuits. In case of problems, or for diagnostic purposes, a matrix of the leakage current flow paths is established by the software before the switching off and the grounding of the system.

System requirements

Considering the circuit characteristics described in table 1, the two operating modes and the test sequence requirement, the following technical parameters for the HVQ system have been targeted during the design phase.

Table 2: HVQ system technical parameters.

Parameter	Unit	Min.	Max.
Number of channels	-	16	80
D.c. voltage	V	0	2000
I charge	μA	1	100
I leak measured	nA	1	1.6·10 ⁻⁶
Voltage ramp rate	V.s ⁻¹	2	255
Temperature	°C	10	40
Relative humidity	%	30	60
Cycle duration	s	30	500
Operation mode	-	continuous	

Detection of current flow paths

By gathering all the information about currents flowing from the energized channel to the inactive ones, it is possible to reconstruct the pattern of the leakage current flow paths. This method allows recognizing the direction of the leakage currents path between all circuits. The measurements are done automatically. Compared to a similar measurement done manually it limits unsafe human interventions on the live part of energized circuits. When one channel is energized by the voltage source, all other channels are connected to the earth of the test system. Each output channel is equipped with a series resistor measuring the return current flow. The principle of the measurement is shown in figure 1.

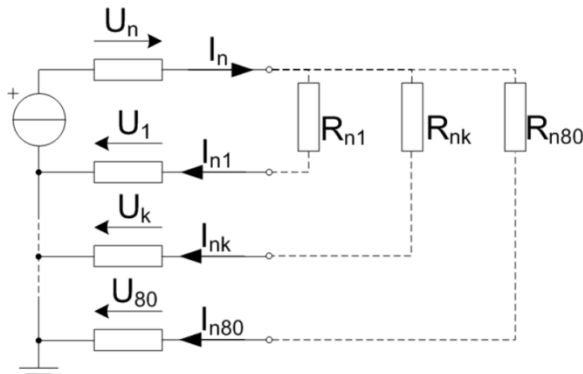


Figure 1: Principle of current flow path detection.

The data acquisition scans the voltages U₁ to U₈₀ while the voltage source remains connected to the tested channel U_n. This allows to measure not only the current I_n that is flowing from the energized channel to the insulation faults but also to measure the currents I_{nk} through the series resistors of each channel. Equation 1 gives the relation between n and k.

$$\sum_{k=1}^{n-1} I_{nk} + \sum_{k=n+1}^{80} I_{nk} = I_n \quad (1)$$

Figure 2 shows the map of the absolute values of the leakage current flow paths gathered between 5 circuits sharing the same cable.

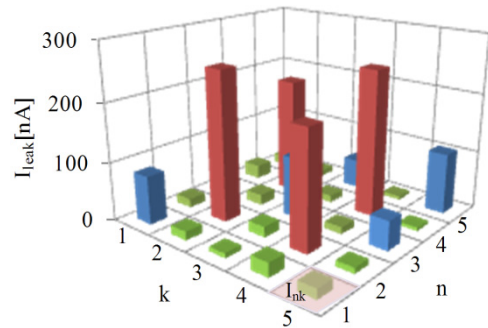


Figure 2: Current flow path matrix.

TECHNICAL DESIGN

The hardware design

The main objectives for the HVQ system design have been the limitation of the internal leakage current, and to avoid internal partial discharges. This is done by applying a specific galvanic insulation design on all elements. All high voltage components are selected for their high breakdown voltage across active parts, typically higher than 2500 V with a minimum insulation resistance of 10¹² Ω. The inter-pin creep distance is another vulnerable point. To avoid creep, dedicated openings are machined in order to increase the distances of the surface leakage current paths between soldered pins. As shown in figure 3, the system is composed of an industrial high voltage power supply, a control and data acquisition card, up to 5 high voltage switching modules and two internal busses, one for control and one for high voltage signals.

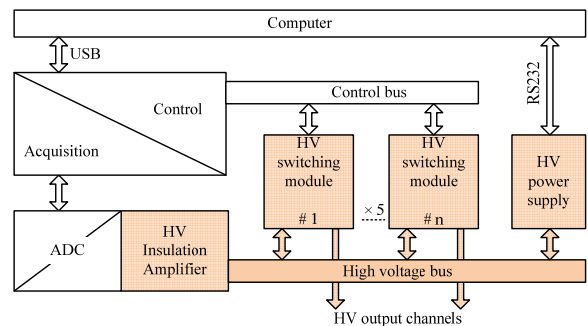


Figure 3: System architecture.

The control and data acquisition card uses an inexpensive PMD-1208LS unit that is equipped with a USB interface. The control offers 8 single ended 10 bit ADC channels and two 8-bit digital ports. The acquisition collects the analog measurements and provides a reliable galvanic insulation of the gathered signals by using AD210BN high precision insulation amplifiers. Each switching module is based on a dual 8-channel structure. Each of the 16 channels contains one reed relay with one type C high voltage switch that allows keeping the corresponding channel to the reference potential when not selected. The voltage drops across the high precision resistors allow the measurement of the leakage currents. This floating voltage measurement is multiplexed on any of the 16 channels by a 2-pole high voltage relay.

Software design

A dedicated LabView library has been developed providing a set of specific high level Virtual Instruments (VIs) capable of controlling all the functions of the HVQ hardware. Two software applications with dedicated interfaces have been created according to the two operating modes.

For the first operating mode, the software is designed for testing a specific LHC circuit. It therefore takes into account the parameters of the circuit, the parameters of the test and in particular the voltage test levels that depend on the status of the superconducting circuit. All test parameters and measured data are available or stored in an Oracle central database server. In order to work offline in areas where technical networks are not available, a local database is used. Whenever the network is accessible, the locally stored data are transferred to the database server.

For the second operating mode the software is designed for the electrical insulation monitoring during the cool down and warm up phases of the LHC machine. In this case the software drives a cycle sequence by testing up to 80 selected electrical circuits. This application requires a network connection and is designed to work continuously without any supervision for periods longer than 3 weeks. During a cycle, the data are stored in a local database and between two cycles the data are sent to the central data base. For this operating mode several current leakage threshold levels can be defined. SMS and e-mail alert messages are dispatched when a failure is detected. The typical data flow diagram is visible in figure 4.

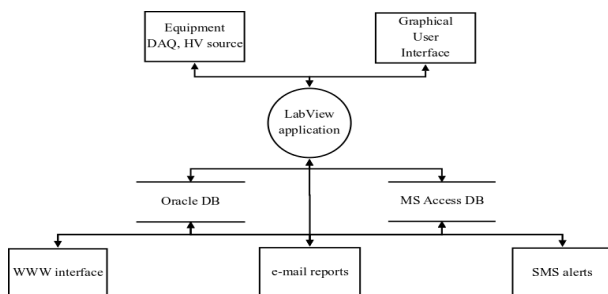


Figure 4: Data management flowchart.

For both operating modes, the software is able to handle problems related to power failures and data transfer software hang-ups without compromising the measurement taken.

EXAMPLE OF MEASUREMENT

Detection of partial discharge to ground

Figure 5 shows a typical example of a partial discharge to ground detected with the HVQ system on a superconducting LHC circuit. The profiles of the applied voltage and of the measured current leakage are shown. The first phase of the chart shows a normal voltage ramp up phase where the charging current is controlled by the system to be lower than 100 μ A. The second phase shows the behaviour of the voltage and the current when the partial discharge to ground of the tested circuit appears.

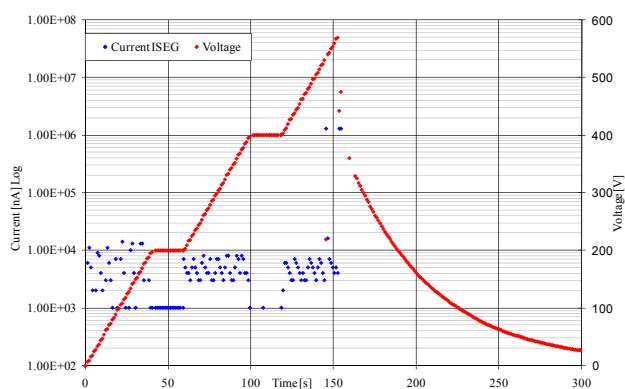


Figure 5: Partial discharge to ground detection.

The recognition by the HVQ system of a partial discharge is done by the read out of three sequential leakage current points above 1 mA. The power supply is switched off and the discharge of the circuit is done through an internal discharge resistor.

CONCLUSION

In total 17 high voltage qualification systems have been constructed and extensively used during the LHC hardware commissioning phase [2]. For both operating modes the system has proved a high reliability by performing on average more than 3200 high voltage switching commutations per installed relay and by working continuously for periods longer than 3 months without failures.

REFERENCES

[1] O. Bruning et al., "The LHC Design Report", Vol. 1, chapter 7, pp 155-216, CERN, 4 June 2004.
 [2] S. Russenschuck et al., "Electrical Quality Assurance of the Superconducting Circuits during LHC Machine Assembly", EPAC 08, 23-27 June 2008.