STABILIZATION OF A KLYSTRON VOLTAGE AT 100 PPM LEVEL FOR PAL XFEL

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Abstract

The PAL XFEL needs a stable electron beam. The stable charging of PFN (pulse forming network) of a klystron-modulator is essential to provide the stable acceleration field for an electron beam. For PAL XFEL, stabilization of klystron voltage pulses at 100-PPM level is required. Short-term stability is determined by a minimum resolution of a charging system. Long-term stability is determined by a thermal stability due to the temperature drift. This paper shows details of hardware R&D and test results to achieve the target stability.

INTRODUCTION

PAL XFEL is proposed as a 4th generation light source that is a coherent X-ray free electron laser by utilizing an existing 2.5-GeV linac [1]. Reasonably stable SASE output requests the RF stability of 0.02% rms for both RF phase and amplitude [2]. This is one of technologically challenging issues for PAL XFEL.

The smart modulator driving a klystron RF source for PAL XFEL will use an inverter charging system. Therefore, the stability of RF sources is directly determined by the one of inverter power supplies. In order to stabilize the charging level, we need an ultra fine inverter power supply and a correct feedback signal of the charging voltage. The proper conditioning of feedback signal with a thermally stable probe is necessary to realize an ultra stable charging performance. This paper shows the hardware development and analysis of the charging stability.

INVERTER CHARGING SYSTEM

A traditional klystron-modulator adopts the resonant charging scheme that uses a constant voltage source. A charging scheme that uses a constant current source such as a inverter power supply provides high reliability: a thyratron switch is safely turned off because next charging schedule is digitally controllable, it is fail-safe system under short-circuit condition due to the current limit feature. In addition, it is naturally compact by using a high frequency inverter [3]. These features are well matched to the next generation modulator for PAL XFEL facility. Figure 1 shows the circuit diagram of a modulator adopting an inverter power supply as a PFN charging power supply. Table 1 summarizes the parameters of a modulator that will provide ultra stable pulses to a klystron (model: Toshiba E3712).

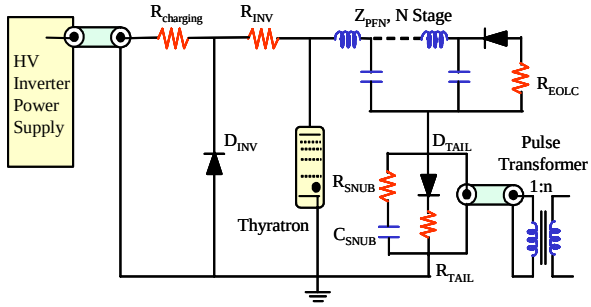

Figure 1: Circuit diagram of a modulator adopting an inverter power as a PFN charging power supply.

Table 1: Modulator specifications

Peak power	160 MW
Peak output voltage	370 kV
Pulse repetition rate	60 Hz
Pulse width	4.7 μs
Pulse energy	750 J
Flat-top width	1.7 μs
Pulse transformer turn ratio	1:17
PFN impedance	2.9 Ω
PFN capacitance	0.8 μF
Main charging inverter	60 kJ/s
Fine charging inverter	2.3 kJ/s
Maximum charging voltage	50 kV

This modulator is to be used for a new facility (fs-THz beamline) of PAL [4], which requires equivalent stability as the one of PAL XFEL. Therefore, this modulator is good test bench for the hardware R&D of the inverter charging system with 100 PPM stability for PAL XFEL.

Figure 2 shows the schematic diagram of the klystron-modulator control including coarse inverters, a fine inverter, a RF driver, a klystron, a thyratron switch of the modulator, a digital inverter controller, a high voltage probe, and a master timing controller (DG535). All the charging inverters are connected to the PFN in parallel. The fine charging inverter has special features that can control the amount of charges per switching cycle to control the regulating ripple of a charging voltage.

Figure 3 shows the timing diagram of a modulator control. The master timing controller provides a charge signal (DG535_A) for inverter power supplies, a thyratron trigger (DG535_B), and a driver trigger for a klystron RF input. The digital inverter controller provides RUN/STOP signals for coarse charging and fine charging.

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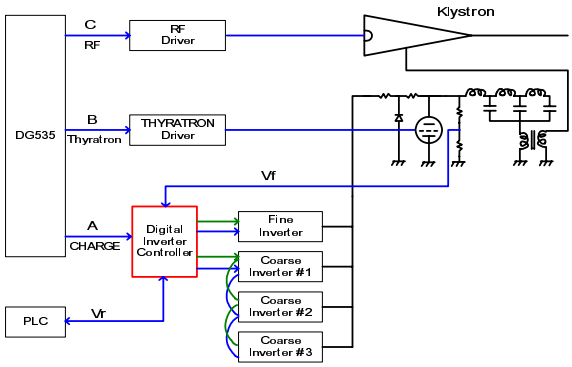


Figure 2: Schematic diagram of the modulator control.

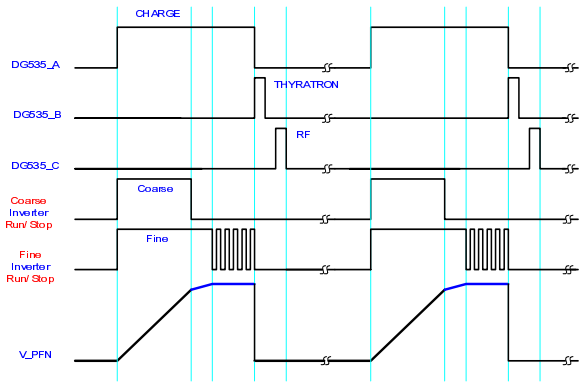


Figure 3: Timing diagram of the modulator control.

The coarse charging level is determined at about 99% of the target charging level. The fine charging unit will charge and regulate the final charging voltage. The increment of the PFN charging voltage per inverter switching cycle, ΔV_{PFN} is given by

$$\Delta V_{PFN} = I_{dc} / (C_{PFN} f_{SW}) = V_{PFN} / (T_C f_{SW}) \quad (1)$$

where I_{dc} is an average charging current, C_{PFN} is a PFN capacitance, T_C is a charging time and f_{SW} is a switching frequency. We have to reduce charging current or increase switching frequency in order to make the charging step small. The charging current has to be large enough to charge the PFN to the target level within the charging time limited by a pulse repetition rate. The switching frequency is also limited to less than 100 kHz due to the switching loss of the solid state devices used in the inverter. Therefore, the PFN charging voltage stability is usually around 0.1% for 100 Hz operating condition. Figure 4 shows typical example of the regulation waveform of a standard inverter, which results 35.6 V fluctuation that is equivalent to 790 PPM at 45 kV with the PFN capacitance of 1.4 μF and a average charging current of 1.8 A.

The charging voltage is not rising smoothly and monotonically but includes high-frequency spikes. The spike is made by the circuit components connected in parallel to the pulse transformer [5]. The noisy spikes have to be removed for the feedback circuit to correctly compare the charging level with a reference level.

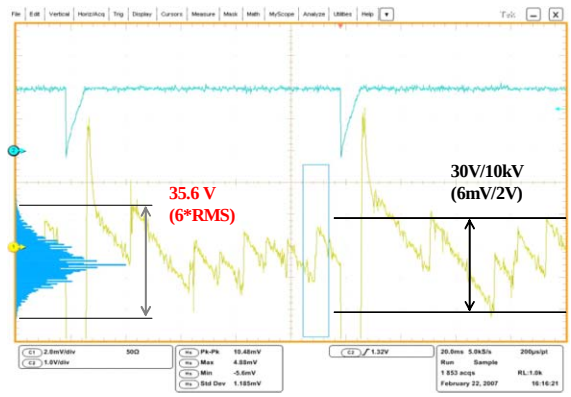


Figure 4: Regulating waveform of PFN voltage at the level of 10 kV with a PFN capacitance of 1.4 μF. The accumulation time for statistical distribution of PFN voltage is 1 hour.

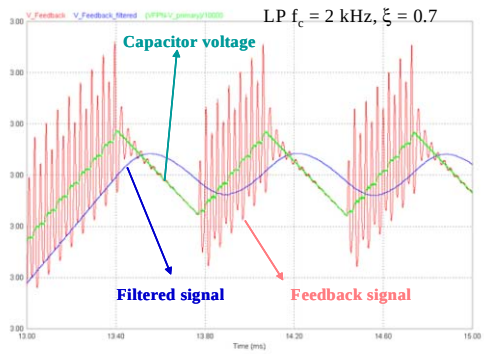


Figure 5: Detail structure of charging regulation.

The conditioning of a feedback signal removes the spiky component by the low-pass filter given by

$$H(s) = \frac{\varpi_o^2}{s^2 + 2\zeta\varpi_o s + \varpi_o^2} \quad (2)$$

where ω_b is a cut-off frequency and ξ is a damping factor. However it results phase delay of feedback signal. This causes the limitation of fine regulation of the charge level as shown in Figure 5 that shows the detail structure of charging regulation. The signal is filtered with a cut-off frequency of 2 kHz and damping factor of 0.7.

DIGITAL INVERTER CONTROL

In order to overcome the phase correction difficulties of an analog feedback, we adopted a digital controller. The digital controller naturally requires a digital reference command for a charging level of the PFN. This condition is good fit to the upper level control system for the communication. It is also useful to keep a stable reference free from any thermal drift and harmful noise. A DSP-based digital controller is developed for the realization of highly stable inverter charging system. This controller has a high-resolution 18-bit ADC (AD7634) and a high-speed

DSP (TMS320F2811). Optical fibbers are used for the interfaces to the inverters to be free from the noise.

The measured value of the PFN Voltage by the digital controller is checked by the DAC output as shown in Figure 6. The built-in software filter with cut-off frequency of 1 kHz makes the signal delay of 0.45 ms that is close to the rise time of 0.35 ms due to the bandwidth of the feedback system. Therefore, the filter has to be included to reduce the noise but a reasonable bandwidth has to be provided to provide less phase delay of feedback signal.

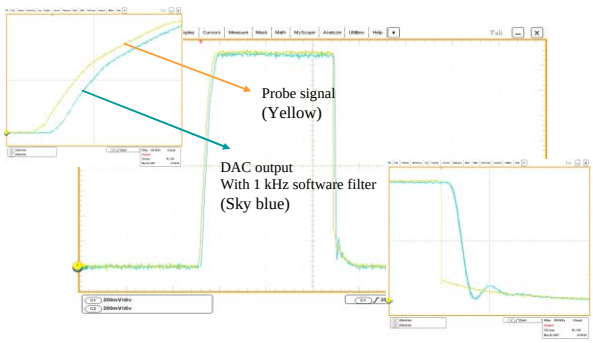
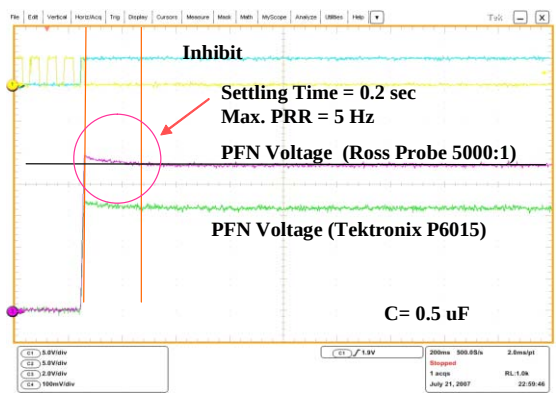
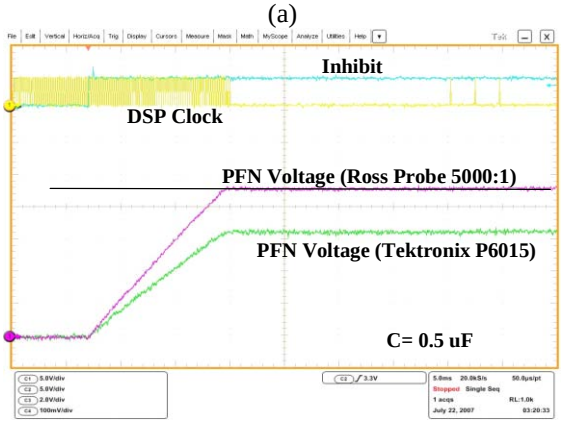


Figure 6: Effect of a digital filter at the charging level of 7.2 kV. The left is fast charging portion of PFN. The right is falling portion at the thyratron switching time.

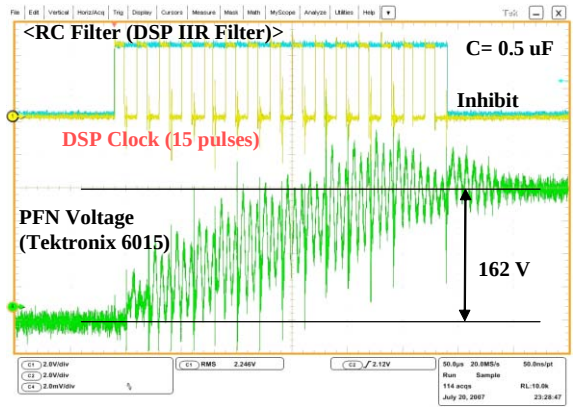


(a)

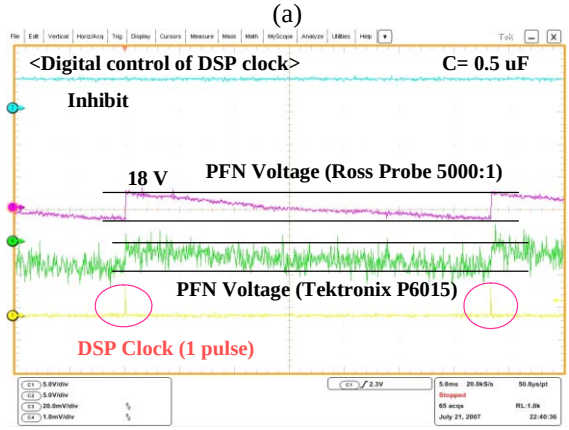


(b)

Figure 7: Digital control of charging overshoot. (a) The charging is done with a digital filter. (b) The charging is done with digital control of a charging pulse rate.



(a)



(b)

Figure 8: Digital control of charging regulation. (a) The charging pattern shows multiple current pulses with a digital filter. (b) Digital control of DSP clock permits only one current pulse per each step.

There is also a certain amount of overshoot due to the phase delay of the digital filter as shown in Figure 7-(a). Even a small overshoot, it takes long time to return to the target level within the 100 PPM error, which is enough to limit the pulse repetition rate, for example, 5 Hz in this test. By digitally controlling the pattern of charging pulse rate near the target level, we can charge the PFN smoothly without losing a charging time as shown in Figure 7-(b).

Due to the same reason, the overshoot also makes the regulation poor at the target charging level as shown in Figure 8-(a). There are 15 DSP clocks corresponding to the charging command for an inverter switching in case a digital filter is used. We already know that one charging pulse is enough to recover charging level. Therefore, one charging command is only permitted then next pulses are blocked for a while. After suitable settling time, we can correctly see the charging level that is to be compared with a target level as shown in Figure 8-(b).

Further improvement of the charging regulation is done by reducing the size of a bucket. PWM (pulse width modulation) is a typical method for the bucket size control. After PFN voltage reaches the target level, charging revel is regulated by smaller bucket with PWM mode.

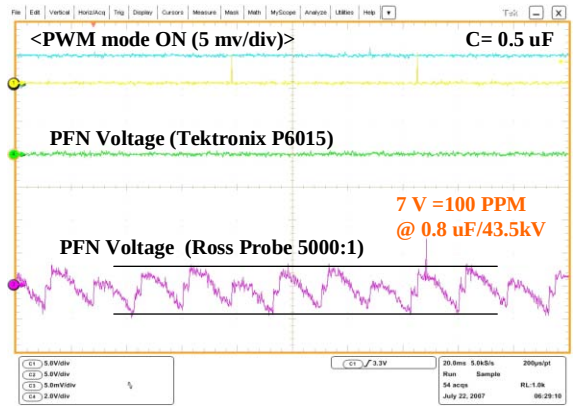


Figure 9: PWM mode and charging regulation.

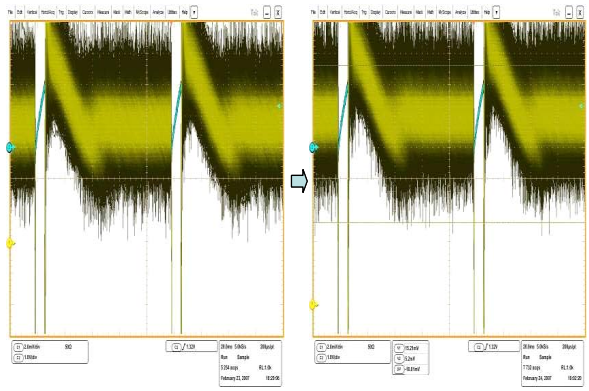


Figure 10: Long-term drift of the PFN charging voltage around 10 kV during 14 hours.

Figure 9 shows the effect of PWM mode on the regulation of charging level. Turning on the PWM mode improves the regulation down to 7 V as shown in Figure 9, which is corresponds to 100 PPM regulation at 45 kV.

PROBING SYSTEM

We need a high voltage probe to measure and feed back the PFN voltage to a controller. A compensated resistive divider is typically used as a high voltage probe. For the stable measurement, the constant division ratio of the probe insensitive to the temperature variation is essential. However the high voltage resistor is temperature sensitive due to the thermal variation of resistance value. Figure 10 shows the mean drift of the charging voltage around 10 kV during 14 hours. It is equivalent to 500 PPM at the 50 kV level. Therefore, we have to use a precision resistor having less temperature coefficient or keep the temperature of the probe body constant by using some temperature control devices such as a Peltier element.

SUMMARY AND DISCUSSION

The charging resolution is determined by the minimum size of charging bucket and the frequency response of a feedback circuit including a probe. The inverter charging system with 100 PPM stability is possible with following considerations. (1) Inverter charging system can meet the short-term stability by choosing both a suitable minimum resolution of a charging system and correct signal conditioning. (2) Long-term stability can be provided by a high precision resistor or a temperature control device of the probe. (3) The residual slow drift can be corrected by adjusting the reference command of the PFN charging voltage in order to provide constant RF amplitude.

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