THE DEVELOPMENT AND APPLICATIONS OF THE DIGITAL BPM SIGNAL PROCESSOR AT SINAP*

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Abstract

A Digital BPM signal processor has being designed in SINAP since 2009. It is a general platform that can be used for the signal processing of a variety of BPM, like stripline BPM, cavity BPM and button BPM. After years of optimization, the DBPM has been used massively on DCLS and SXFEL. And the turn-by-turn resolution of the storage ring DBPM on SSRF is 0.34μ m. This topic will introduce the development and applications of the DBPM at SINAP, also the future DBPM development for next generation light source will be discussed here.

INTRODUCTION

BPM is an important diagnostic instrument in accelerator. It provides the beam position in tunnel, which can be used for accurate beam control and other beam parameters measurements. There have a variety of BPM sensors for different occasions on accelerator, such as stripline BPM, button BPM, cavity BPM, shoebox BPM, et.al. Except for the sensor, the BPM signal processing electronic is a key component of the BPM system. The signal processing system can mainly including RF signal conditioning, ADCs digitizing analogue signal into digital signal, FPGA processing digital signal and calculate the beam position, data acquisition in CPU sending out the results and communicating with control center through LAN. Figure 1 is the block diagram of BPM signal processing system.



Figure 1: BPM signal processing system.

BPM sensors are installed at the concerned place of the accelerator, larger accelerator always containing more BPMs. For example SSRF is a 432m electron storage ring and contains about 200 BPMs, and future Shanghai Hard X-ray FEL will have more than 200 BPMs along the 3km facility. Since 2009, SSRF started the development of DBPM processor, the objective is to develop a stand-alone general hardware platform that can be used for diverse signal processing applications on accelerator. The first version DBPM completed at about 2011, and lab-tests and on-line beam tests have been carried out. The results shown that the turn-by-turn data resolution can be better than 1μ m, and the 10Hz SA data can be read correctly [1]. After five years' optimization, a second version DBPM has been designed and firstly made mass field application on DCLS and SXFEL, and small amount DBPMs is under test on SSRF.

The DBPM specification is listed in Table 1.

Table 1: DBPM Specifications

Parameter	Value
Channels	4
Central Frequency	500MHz
Bandwidth	~20MHz
Dynamic range	31dB
ADC bits	16
ADC bandwidth	650MHz
Max ADC rate	125MSPS
FPGA	Xilinx xc5vsx50t
Clock	Ext./Int.
Trigger	Ext./Self/Period
Software	Arm-Linux/EPICS

Figure 2 is the architecture of the processor. RF conditioning and ADCs are located on RF board, others on digital carrier board. Figure 3 is the hardware of RF board and digital board.

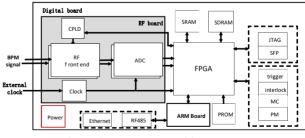


Figure 2: Processor architecture.

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APPLICATIONS ON FEL

The DBPM is made mass field application (about 80 sets) firstly on two FEL facilities in China, DCLS and SXFEL[2], both accelerators are constructed by SINAP. The FEL contains two types of BPM, stripline BPM and cavity BPM. The stripline BPM signal is processed directly with DBPM, while the cavity BPM signal (about 4.7GHz) is down-converted to 500MHz firstly before into the DBPM. Figure 4 is the field picture of DBPM cabinet and the control panel in center room.

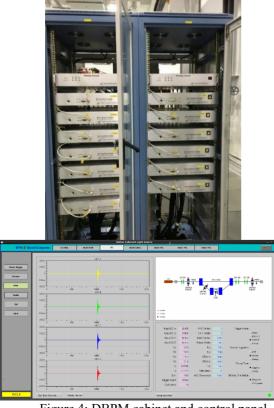


Figure 4: DBPM cabinet and control panel.

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On first version, both stripline and cavity BPM signal processing algorithms are implemented in EPICS IOC on ARM, including Hilbert and FFT. The complicated software consumes too much ARM computing power, can only meets the operation under 10Hz bunch rate. However, DCLS and FEL plan to run at 50 bunch rate in future. At the bottom of 2017, the signal processing algorithms are implemented in FPGA, and whole firmware and software are upgraded. The signal processing power is greater than 100Hz bunch rate now.

The performance evaluation is carried out on DCLS by feeding two DBPMs with divided BPM (or IF) signal. Figure 5 is the RMS resolutions of stripline DBPM and Cavity DBPM at different bunch charge. The RMS of stripline DBPM and cavity DBPM at 500Pc is about 2.27µm and 0.54µm respectively.

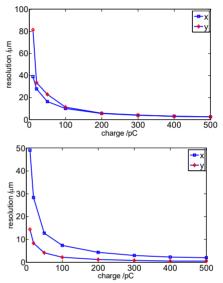


Figure 5: RMS of Stripline DBPM (up) and cavity DBPM (down).

The cavity BPM k factor is measured by moving the BPM. Figure 6 is the result of horizontal k factor of CBPM7 at DCLS. The k is about 0.37 after linear fitting.

The beam direction of cavity BPM is judged by measuring the phase difference between position cavity and reference cavity. There may have 2π phase jump in one direction that needs correction. Figure 7 shows the phase correction and the phase jump between two directions.

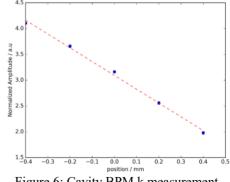


Figure 6: Cavity BPM k measurement.

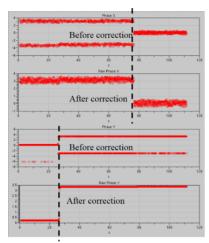
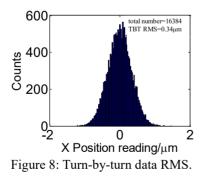


Figure 7: Cavity BPM phase.

APPLICATIONS ON SSRF

The new DBPM for SSRF storage ring has been tested at the Jan. of 2018. The tests including resolution evaluation and accuracy check with Libera Brilliance. There have a spare BPM at 11 unit. A pickup signal is divided into 4 and put into a DBPM to measure the RMS resolution, the data RMS of turn-by-turn (16384 samples), FA50kHz (1171 samples) and FA10kHz (235 samples) is $0.34\mu m$, $0.15\mu m$, $0.09\mu m$ respectively. Figure 8 shows the TBT resolution.

Signals from BPM four pickups are divided and put into DBPM and Libera Brilliance to check the accuracy (assuming the measurements of Libera Brilliance are accurate). Figure 9(up) is the spectrum of TBT data, two lines fit quit well. Figure 9(down) is long time SA data of Libera Brilliance and DBPM. There have obvious difference between them before correction. The difference is introduced by current dependency of DBPM, which comes from the difference between four channels. Curve fitting algorithm is applied on the four channels to eliminate the effection. It shows that two lines fits quit well after correction.



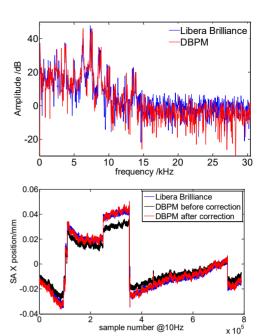


Figure 9: Comparison between DBPM and Libera Brilliance, TBT(up) and SA(down).

OTHER PROCESSORS

Except for the developed DBPMs mentioned above, the SINAP is developing other higher performance processors. One is bunch-by-bunch DBPM, some good results have achieved [3]. Another is RF-sampling processor, which can digitize the RF signal of cavity BPM directly [4]. The signal processing system on FEL will be improved greatly by applying the RF-sampling processor.

CONCLUSION

A general DBPM has been developed at SINAP by developing different firmware and software on same hardware for different applications. The DBPM have made mass on-line application on DCLS and SXFEL, and already made long time evaluations on SSRF, the TBT RMS is $0.34\mu m$ and SA results fits well with Libera Brilliance, it can be used for future replacement.

REFERENCES

- Lai Longwei, Leng Yongbin, Yi Xing, et.al. "Optimization of signal processing algorithm for digital beam position monitor (in Chinese)", High power laser and particle beams, Vol. 25, No. 1, Jan. 2013 pp.109-113.
- [2] L.W. Lai, Y.B. Leng, Y.B. Yan, et,al. "Design and Performance of Digital BPM Processor for DCLS and SXFEL", proceedings of IPAC2017.
- [3] Yongbin Leng , Zhichu Chen, Longwei Lai, et.al. "Bunch by bunch DBPM processor development and preliminary experiment in SSRF", Proceedings of IPAC2015, Richmond, VA, USA, p. 984-986.
- [4] L.W. Lai, Y.B. Leng, J. Chen, et,al. "The Application of direct RF sampling system on cavity BPM signal processing", Proceedings of IBIC2017, Grand Rapids, Michigan, USA.