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THE DIGITAL CONTROLLER FOR POWER SUPPLIES IN HIAF*

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Abstract

High Intensity Heavy Ion Accelerator Facility (HIAF) is a project proposed by Institute of Modern Physics, Chinese Academy of Sciences (IMP). This paper designs a digital controller for Bring in HIAF dipole power supplies system, which is several circuit boards consist of high precision ADC, optical fiber module, DDR3 SDRAM, Gigabit Ethernet module. It uses Cyclone V SX SoC FPGA, which integrated with dual-core ARM Cortex-A9 MP Core processor. This paper explains the hardware and software architecture of the controller and how can it improve power supplies performances. The FPGA finishes the PI regulating and PWM modulation. The ARM is responsible for data pre-setting, web service, database, and power supplies detection and protection management. At the end, this paper gives the output measurements when the controller is used in the prototype, which verifies the rationality and reliability of the design.

INTRODUCTION

HIAF [1] is a new facility for heavy ion researches [2], which consists of two ion sources, a high intensity Heavy Ion Superconducting Linac (HISCL), a 45 Tm Accumulation and Booster Ring (ABR-45) and a multifunction storage ring system. Because the Booster Ring has high quality requirement for beam, the power supplies for magnets should have high stability, reliability, and small tracking error, small current ripple. This paper describes a controller which is designed for Booster Ring dipole power supplies. The aim of the new controller is to improve the real-time performance, stability, and reliability.

HARDWARE ARCHITECTURE

This part describes the chip selecting of the controller and the main boards. Some papers have proposed the design of a new controller [3] uses Raspberry Pi and FPGA, which means that ARM and FPGA have both used in accelerator power supplies area. Further, this paper proposes SoC FPGA which integrates ARM and FPGA, which makes the design more reliable because of the simplicity.

Chip Selecting

The controller uses Cyclone V SX SoC FPGA, which has the main performance as: Hard memory controllers supporting 400 MHz DDR3 SDRAM with optional error correction code (ECC) support, PCI Express with multifunction support, variable-precision digital signal processing (DSP) blocks, and HPS Dual-core ARM Cortex-A9 MP Core processor. In controller, it has DDR3 SDRAM, FLASH, fiber optic 88e1111, and Ethernet module. What the old one used is Cyclone II FPGA EP2C70 [4]. The differences of two FPGA resources between two controllers are listed as Table 1. The change of the chip can improve the speed of the controller.

Table 1: The Differences Between FPGAs

Items	Cyclone V	Cyclone II
LEs	68,416	110,000
Pins	499	422
Memory bits	5,662,720	1,152,000
DSP blocks	112	/
Multipliers	224	150
Total PLLs	15	4

Main Boards

Figure 1 shows that the controller has 5 boards, which consists of main board, mother board, ADC board, extended board, and PLC board. All these boards use high speed protocol to communicate with each other. GXB is used between mother board and ADC board. Except for GXB, this controller also uses industrial general protocol such as RS232, RS485, and CAN. The old controller [4] has 7 boards, including the boards the same as the new one and MCU boards, power board. Giving up redundant boards makes the system be more reliable.

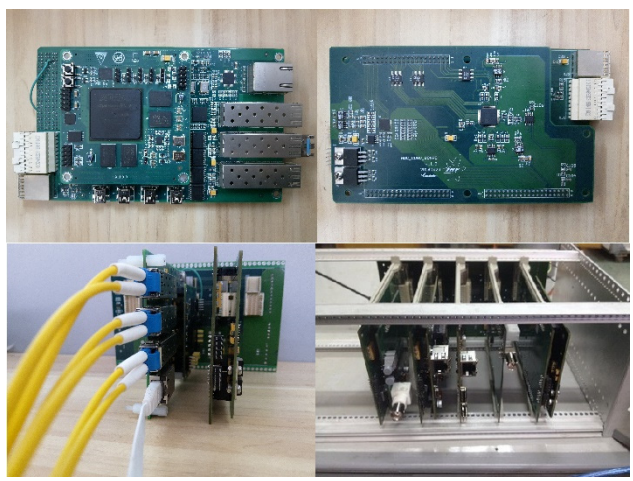

Figure 1: The photos of the controllers.

SOFTWARE ARCHITECTURE

The software architecture of the controller has two parts, which is FPGA and ARM. The FPGA part uses Verilog

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HDL language to finish parallel program, and the ARM part which is embedded Linux uses C language for programming.

FPGA Part

The FPGA finishes the PI regulating and PWM modulation. FPGA is also responsible for communicating with PLC, and receiving some states such as overcurrent fault, overvoltage fault, interlock fault. Compared to the old one, the new controller using new series FPGA can be more flexible to finish some power on self-tests cooperating with ARM. And the greater memory resources make storage be more convenient.

ARM Part

The ARM is responsible for data pre-setting, web service, database, power on self-tests, and power supplies detection and protection management. To be real timing, the controller adopts White Rabbit timing System. All the read-back data have timestamps, which is convenient for the physicist to regulate beam. In the ARM, it runs an embedded real-time Linux. Compared to the old controller, it makes full use of Linux, and gives up the shortages of NIOS II.

The Communication Between FPGA and ARM

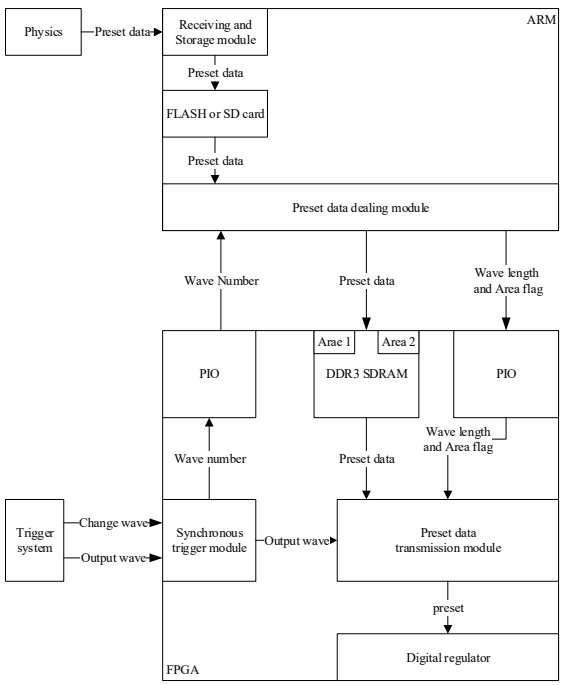

Figure 2: Pre-set data transmission flow.

The Hard Processor System (HPS, also called ARM) and FPGA communicate with each other through bus interfaces that bridge the two distinct portions. There are three bridges between HPS and FPGA, which are FPGA-to-HPS Bridge, HPS-to-FPGA Bridge, and Lightweight HPS-to-FPGA Bridge. This design uses HPS-to-FPGA Bridge to finish pass pre-setting data from ARM to FPGA. Except for that, Lightweight HPS-to-FPGA Bridge is used to transmit some enable signals and flag signals through PIO to make sure the sequential between two parts is synchronous. The details about how the pre-set data transmits are listed as Fig. 2. And it uses FPGA-to-HPS Bridge to finish passing read-back data including currents, voltages, and states from FPGA to ARM DDR3 SDRAM, which is shown in Fig. 3. All these read-back data can be saved into file on SD card.

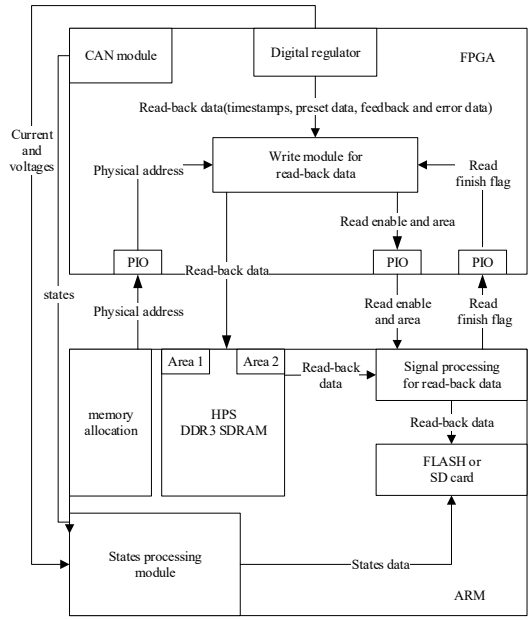

Figure 3: Read-back data transmission flow.

RESULT

Figure 4 gives the photos of debugging. The controller is used to control the prototype whose loads are quadrupole magnets, and the measurements screenshots from oscilloscope about output current is shown as Fig. 5 and Fig. 6.

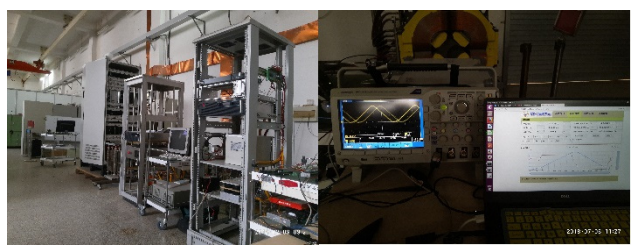

Figure 4: The photos of debugging.

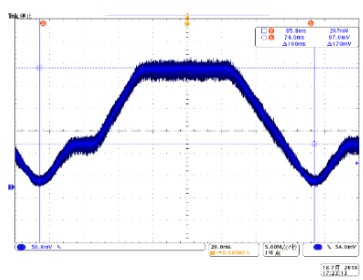

Figure 5: Oscilloscope screenshots (pulse current output, maximum current 15A).

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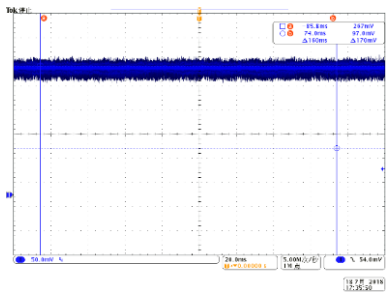

Figure 6: Oscilloscope screenshots (direct current output 15A).

This paper analyses the result from FPGA processing by Python in Linux and draws the error between given and output current as follow. Figure 7 is the data about 15A pulse current output. Figure 8 is the data about 15A direct current output. With the data from direct current output, it can make a conclusion that the stability is 0.05, calculating as Eq. (1). (MaxCur means the maximum output current, and MinCur means the minimum output current.) Because the prototype is 600A, the stability achieves the requirements. The error is lower than ±0.7A (pulse current) and ±0. 0035A (direct current).

$$Stability = \frac{MaxCur - MinCur}{MaxCur + MinCur}$$

$$= \frac{15.75-14.25}{15.75+14.25} = 0.05\,. \qquad (1)$$

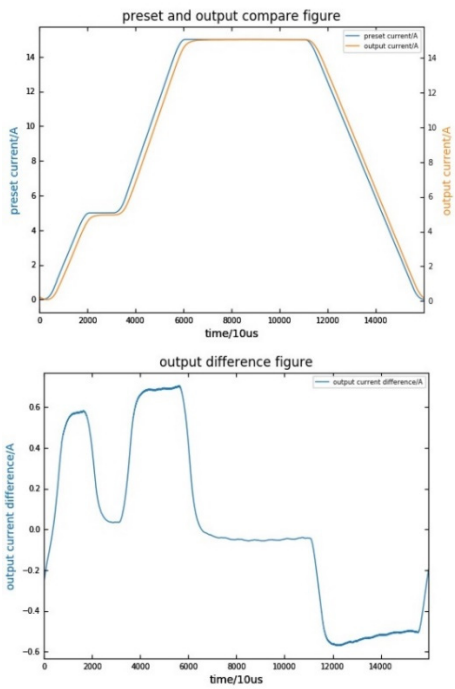

Figure 7: The pulse given and output current (the above one) and the error between given and output (the bottom one).

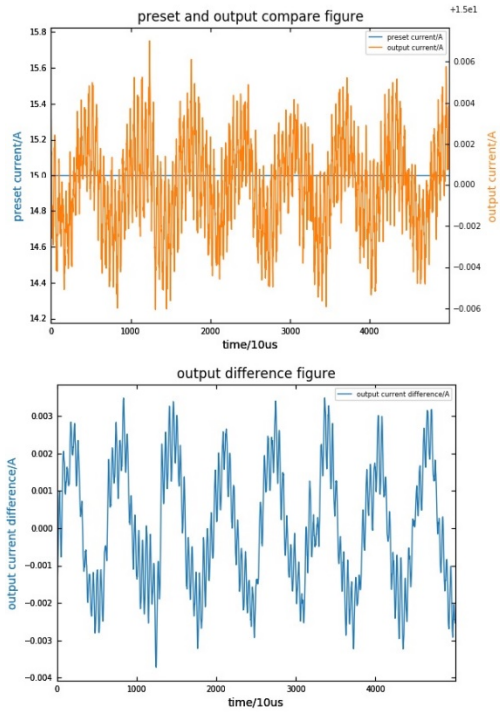

Figure 8: The direct given and output current (the above one) and the error between given and output (the bottom one).

CONCLUSION

This paper gives an architecture of the digital power supplies controller in HIAF. It proposes a new idea about using SoC FPGA in accelerator power supplies field. With reducing the boards number, the controller becomes more reliable. And it makes full use of embedded Linux, which means it can overcome the shortcoming of NIOS II. Finally, testing in prototype proves that this controller is qualified.

REFERENCES

[1] J.C. Yang, J.W. Xia, G.Q. Xiao, *et al*., "High Intensity heavy ion Accelerator Facility (HIAF) in China", Nuclear Instruments & Methods in Physics Research, Vol. 317, p. 263-265 Part: B, Dec. 2013, doi:10.1016/j.nimb.2013.08.046

[2] Shuang R, Yang J, Zhang J, *et al*., "Design of extraction system in BRing at HIAF", Nuclear Instruments & Methods in Physics Research, vol. 892, p. 53-58, Jun. 2018, doi:10.1016/j.nima.2018.02.052

[3] Visintini R, Cleva S, Cautero M, *et al*., "A New Concept of Controller for Accelerators' Magnet Power Supplies", IEEE Transactions on Nuclear Science, vol. 63, Issue. 2, p. 849-853, Part: 2, Special Issue: SI, Apr. 2016, doi:10.1109/TNS.2015.2498480

[4] Zhao J, Gao D, Chen Y, *et al*., "Implementation of an FPGA controller for correction power supplies in heavy ion synchrotron", Nuclear Instruments & Methods in Physics Research, vol. 777, p. 167-171, Mar. 2015, doi:10.1016/j.nima.2014.12.115