MICROTCA.4 BASED OPTICAL FRONTEND READOUT ELECTRONICS AND ITS APPLICATIONS

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Abstract

In the paper the MicroTCA.4 based optical frontend readout (OFR) electronics and its applications for beam arrival time monitor (BAM) and fast beam based feedback (BBF) is presented. The idea is to have a possibility to monitor the modulation density of the optical laser pulses by the electron bunches and apply this information for the BBF. The OFR composed of double width fast mezzanine card (FMC) and advanced mezzanine card (AMC) based FMC carrier. The FMC module consists of three optical channel inputs (data and clock), two optical channel outputs (beam arrival time), 250 MSPS ADCs, clock generator module (CGM) with integrated 2.8 GHz voltage control oscillator (VCO). The optical signals are detected with 800 MHz InGaAs photodiodes, conditioned using 2 GHz current-feedback amplifiers, filtered by 3.3 GHz differential amplifiers and next direct sampled with 16-bit 900 MHz of analog bandwidth ADCs. The CGM is used to provide clock outputs for the ADCs and for the FMC carrier with additive output jitter of less than 300 fs rms. The BAM application has been implemented using Virtex 5 FPGA and measured with its performance at Free Electron LASer in Hamburg (FLASH) facility.

INTRODUCTION

The Micro Telecommunication Computing Architecture (MicroTCA) is a standard in Telecommunication from several years. Nowadays more often high energy physics research centres are trying to migrate from commonly used Versa Module Europa (VME) to more compact, modular, redundant solutions offered by MicroTCA, especially generation four of the standard. The Deutsches Elektronen-Synchrotron (DESY) in Hamburg in Germany is a leading institute which developing, designing, testing and even commercializing general purpose and application specific modules using this modern technology. Moreover, the next generation light sources such FLASH and European X-Ray Free Electron Laser (E-XFEL) accelerators have been decided to be fully controlled and monitored with its crucial parameters by MicroTCA.4 [1].

The scope of the paper is to summarise the several year research and development (R&D) program on developing direct sampling OFR electronics [2]. The OFR electronics have been optimized to get the best achievable performance when considering the optical to RF conversion of the laser pulses, ADC stability and fast data processing by FPGA's. Fast digital feedback information can be sent out using small form-factor pluggable (SFP) optical modules allowing data transfers up to 10 Gbps. The OFR electronics can be efficiently applied for several applications.

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Within the paper we are presenting its usage for BAM and BBF experiments.

BEAM ARRIVAL MONITOR AND BEAM BASED FEEDBACK APPLICATIONS

The BAM signal creation, detection and analysis in the electron bunch arrival time monitor is split into several subsystems, each fulfilling a particular function as shown in Fig. 1.
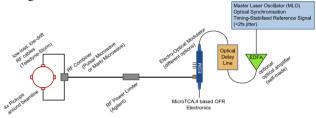

Figure 1: The block diagram of BAM detector.

The RF module which consists of four broadband pickups mounted in the beam tube is applied in order to capture the electric field induced by the passing electron bunches. The signals of opposite pickups are combined for a reduced position dependence of the measurement, resulting in two independent RF channels for the arrival time detection: course and fine. Than the electro-optical modulator (EOM) unit is introduced mainly for translating the RF signals into an amplitude modulation of time-stabilized, ultra-short laser pulses provided by the Master Laser Oscillator (MLO) synchronization system in order to achieve a high temporal sensitivity. The optical frontend electronics need to be installed at the end of the system for signal processing and control of the individual subsystems [3].
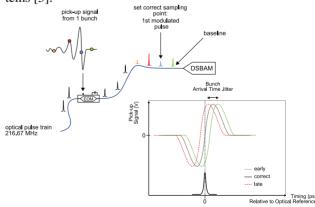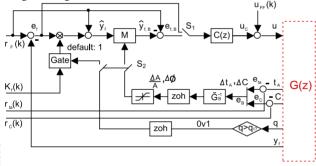

Figure 2: The block diagram of BAM signal detection and calibration.
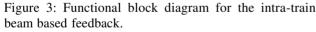
The beam arrival time is calculated using peak and baseline values of the first modulated (mod) and first unmodu-

lated (unmod) laser pulses according to the following formula:

$$BAM = \frac{Peak_{mod} - Baseline_{mod}}{Peak_{unmod} - Baseline_{unmod}}. \qquad (1)$$

The search of the correct BAM signal operating point (zero-crossing region) is done by a change of the position in time of the laser pulses using motorized delay stage (see Fig. 2).

The RF field stability is one of the major components which determine the beam stability. The path to improve this is certainly to use the beam itself as a detection mechanisms and feedback the information to the corresponding RF station. Here one can distinguish between two time scenarios in a pulsed machine. First to compensate for drifts induced to the machine due to environmental influences of other subsystems as well as the regulating RF station itself. The information of the arrival time from the previous pulses can be used to correct the actual one. At FLASH this is meant to be the slow RF feedback. With the current repetition rate this feedback can achieve a maximum frequency of 10 Hz. In order to compensate for stochastically and fast fluctuations appearing from pulse to pulse an intra train feedback is required, acting on the bunches of the same pulse by information of the previous bunches of the same train. Depending on the delay and bandwidth of the feedback system disturbances up to a few hundred kHz can be compensated. In order to illustrate the functionality in Fig. 3 a functional block diagram is given.

Figure 3: Functional block diagram for the intra-train beam based feedback.

The system itself is described as G(z). As an input to the system, the RF drive given as u is a function of the measured RF field y_F and the arrival time t_A. For further details we refer to [4]. Beside the arrival time also the compression signals are processed in the loop which is necessary in terms of coupling between those two signals with the manipulation of amplitude and phase settings of the RF field. Further coupling of arrival time and compression changes between different RF stations along a linac with several bunch compression and drift sections has to be also taken into account. Coupling and distribution of fast feedback data is foreseen.

OFR HARDWARE OVERVIEW

The OFR electronics are composed of double width FMC module and supporting AMC based carrier as shown in Fig. 4 [5]. The DFMC-DSBAM adapter is equipped with 3 optical inputs and 2 optical outputs placed on the front side of the module. The optical inputs are used to provide data and clock signals directly obtained from optical laser pulses. The idea is to provide each of data channel into two independent ADC channels using single-ended to differential buffers. The optical signal conversion to its electrical representation is performed using photodiode and transimpedance amplifier. In order to avoid problems with optical cables mismatch and different length, the programmable attenuators have been introduced. The main concept is to have a possibility to make remote calibration of each of data input channels with respect to the fact that ADC buffers have maximum possible gain. The heart of the system is CGM module that synthesizes optical input clock into 4 LVPECL and 4 LVDS clock outputs. The LVPECL and LVDS clock outputs are grouped into pairs. The each pair is equipped with its individual frequency dividers. In addition LVDS outputs are equipped with ramping capacitors that can be configured for different ramping current values and as a result allowing additional fine delays of each output individually.
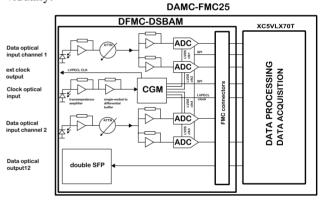

Figure 4: The block diagram of MTCA.4 based OFR electronics.

For the BAM application the optical input clock period is 4.6 ns. The CGM module is than phase locked with 216 MHz input using built-in phase locked loop (PLL) equipped with VCO operated at 2.592 GHz. The direct output of the PLL is divided by 2 giving a possibility to provide 1.296 GHz reference frequency driving one of the LVPECL outputs. Finally each of ADC clock can be shifted by 6 independent coarse steps of 800 ps each. The fine delay allows making 48 individual steps of 16 ps each. The ADC chips have been equipped with self-testing procedures implemented by manufacturer. The proper operation of the chips can be easily verified without any optical signal connection for the data channels. The LVDS data outputs of each ADC are fed to the carrier using both available FMC connectors. The information of operating voltage of FMC module is stored inside field replaceable unit (FRU). The voltage record is read by the

carrier using module management controller (MMC) and then the proper voltage level is adjusted. The each FMC module has its unique identification (ID) number together with sensor data records (SDR) filled out with temperature meters. The raw data from ADCs are processed by the FPGA device ported to DAMC-FMC25 carrier. The data are next sent back to the FMC module using fast serial links connected to built-in multi-gigabit transceivers (MGTs) on the FPGA side and to the SFP modules on the FMC module side.

FIRMWARE AND SUPPORTED SOFT-WARE

The OFR electronics firmware is processing two independent bunch arrival monitor (BAM) channels. The peak and baseline of the optical pulse are digitized by two ADCs. FIFO memories store ADC data using the 216 MHz ADC data clock (DCLK). IODELAY component allows shifting of the input clock to match the data lines from the ADC. The 216 MHz system clock is also applied to the second port of the FIFO. The 1024 data points are stored in the BRAM memory in the FPGA with full 216 MSPS acquisition frequency for PLL delay adjustments. The SYNCH block synchronizes the data from the FIFO to align them with the input TRIGGER and match with the electron bunches. The BAM component uses information from two SYNCH blocks (two pairs of unmodulated and modulated pulses) to compute the bunch arrival time (BAT). Computed BAT is then sent to the RF field controller via a 3.125 Gbps fiber link using the proprietary LLL protocol. The BAT so as the other variables are stored in the data acquisition (DAQ) block for the post-processing with the high level software (HLS). The HLS also provides the configuration parameters by the PCIe bus. Internal registers in the FPGA are addressed using the internal bus (IBUS) [6]. Internal PLL in the FPGA synthesizes the divided 108 MHz clock which is used for components outside of the processing pipeline which do not require low latency operation. The block diagram of BAM firmware is shown in Fig. 5.
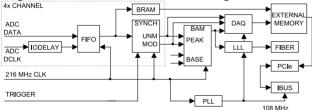

Figure 5: The block diagram of supporting firmware for BAM application.

The BBF firmware first computes the difference between RF field set-point (SP) and vector sum (VS). The resulting field error is scaled by BBF Gain, which is one in case of no beam, otherwise a user defined value. Next the field error is modulated by the beam error (AMP CORR and PHS CORR), which is done around the SP. The beam error is computed from bunch arrival monitor and bunch compression set-points (BAM SP). The beam scaling factor is a part of the transformation matrix whose ele-

ments correspond to the weighting of bunch arrival time and bunch compression measurements, respectively. A limiter for beam related amplitude and phase is implemented to avoid undesired large field changes if one of the beam measurements is corrupted. Within the limits, the input is fed through to the output, while the output is truncated in case of reached predefined limits. Furthermore, the set-point correction is done by a manipulation of the predefined RF field set-point, leading to a beam based correction (BBF error) as shown in Fig. 6.
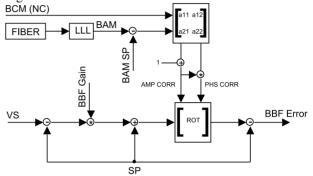

Figure 6: The block diagram of supporting firmware for BBF application.

The high level software for the data acquisition system and slow control is written using the distributed object oriented control system (DOOCS) framework [7]. The state machine for the high level software is show in Fig. 7.
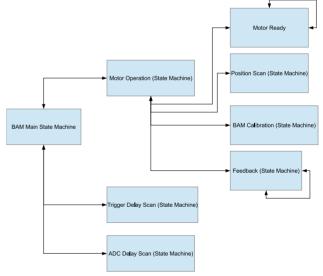

Figure 7: The HLS software state machines to control BAM application.

The default state for the Main State machine is Motor Operation which is as a State Machine as well and the default state for the Motor Operation State Machine is simply Motor Ready. The system remains in this state until an external trigger causes a transition. A transition may occur internally the Motor Operation State Machine to Position Scan or BAM Calibration or Feedback which are State Machines as well. The first is used to find the working point during initialization and configuration of

the BAM system, BAM Calibration to determine the parameters to transform modulation in femtosecond and Feedback to provide slow feedback. The system can remain indefinitely in Feedback state. An external trigger maybe cause also a transition inside the BAM Main State Machine, from Motor Operation to the states Trigger Delay or ADC Delay Scan. Both are State Machines as well and they are used to configure the BAM System.

EXPERIMENTAL RESULTS AND CONCLUSIONS

The OFR electronics have been installed inside 12 slot Schroff MTCA.4 crate at injector hutch in FLASH and connected to 3DBC2 BAM detector located after first accelerating modules (ACC1 and ACC39) but before first bunch compressor. The OFR electronics have been connected with optical fiber cable to LLRF controller of ACC1 module.

The optical laser pulses have been adjusted with their optical power level using laser driver current of 200 mA in order to not saturate the monitoring ADCs. Next the peak and baseline values of the first modulated and none modulated laser pulses have been captured at 14e3 and -5e3, respectively. During the process absolute value calculation (peak minus baseline of the laser pulse) the ADC raw data stability performance has been measured as shown in Fig. 8.
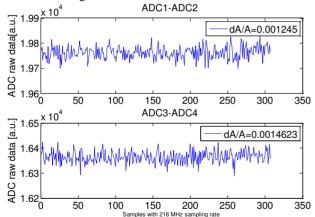

Figure 8: ADC stability measurements for the BAM signals detection of 3DBC2 detector.

Finally, the beam arrival time has been estimated to be of order of 4 ps of the mean value over several tens of measurements. The BBF controller has been setup with its basic functionality excluding bunch compression information (not available yet). During feedback controller operation the rms value of beam time arrival over more than 100 measurements has been recorded for 200 bunches along the bunch train repeated with 1 MHz (see Fig. 9).
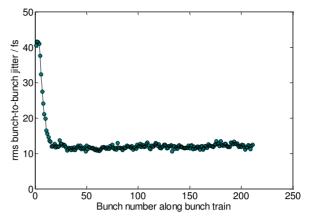

Figure 9: The BAM and BBF application performance at 3DBC2 BAM at FLASH.

The designed OFR electronics have been successfully demonstrated for beam arrival time and fast beam based feedback experiments. The achieved bunch to bunch jitter has been reduced from 40 fs (without BBF) up to 12 fs (with BBF) when considering in-loop measurements (the same detector used as a sensor). The permanent system installation is scheduled and its regular operation supporting beam acceleration efficiency (i.e. SASE) is foreseen.

ACKNOWLEDGEMENT

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