INDUSTRIALISATION OF CAVITY BPMS

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Abstract

The industrialisation project of a cavity beam position monitor (CBPM) has been commissioned aiming at providing reliable and economical CBPM systems for future Free Electron Lasers (FEL) and similar linac-based facilities. The first prototype of a CBPM system was built at Versatile Electron Linear Accelerator (VELA) in Daresbury Laboratory. We report on the measurement results from the first prototype of our system at VELA and current developments of CBPMs, down-converter electronics and Data Acquisition (DAQ) system.

INTRODUCTION

CBPMs have gradually moved from an exotic extreme spatial resolution tool designed for use in final focus collider systems [1] to an FEL workhorse [2, 3] providing sub-micrometre resolutions even at low, typically less than 100 pC bunch charge. An industrialisation project had been started jointly by the John Adams Institute (at Royal Holloway, University of London), FMB-Oxford and Daresbury Laboratory in 2014 with support by the Science and Technology Facilities Council (STFC) Innovations Partnership Scheme (grant number ST/L00013X/1). The aim of the project is to design a low-cost, easy in operation and reliable CBPM system that could be deployed even in smaller high brilliance light facilities with no direct access to the required expertise.

A basic CBPM system typically consists of 2 cavities: one position (dipole) and one reference (monopole) cavity for charge and phase normalisation, a set of down-converter electronics, high-speed digitisers for data acquisition and digital processing. In order to kick-start the project, cavity, electronics, DAQ and processing development, as well as setting up the beam experiment started in parallel, with an existing cavity [4] used as a test subject to set up the beam measurements while the new cavities are still in development. The beam test has been set up at STFC Daresbury Laboratory in VELA test facility.

CBPM TEST SYSTEM AT VELA

We built the first prototype of CBPM system at VELA in Daresbury Laboratory. Currently, the system includes one position and one reference cavity, and is planned to be extended to 3 position cavities plus reference in 2017. There are 2 precision position stages moving a single CBPM horizontally and vertically with respect to the beam (Fig.1). The motion stages are controlled remotely via a MINT motion controller coupled with a PC running LabVIEW code. Three channels of homodyne down-converting electronics reduce the frequency of the signal down to about 20 MHz (Fig. 2).

Two Red Pitaya [5] open source SoC (system on a chip) boards are deployed for DAQ. Red Pitaya hosts a single processor plus FPGA (field-programmable gate array) chip, two 125 MHz 14-bit ADC and 2 DAC channels and a number of GPIO pins. The native code has been modified in order to acquire signals with external trigger and include EPICS (Experimental Physics and Industrial Control System) API modules for seamless interfacing with VELA for DAQ and control.

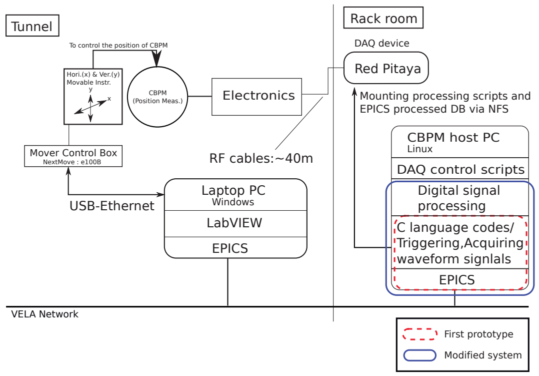

Figure 1: The layout of CBPM system in VELA.

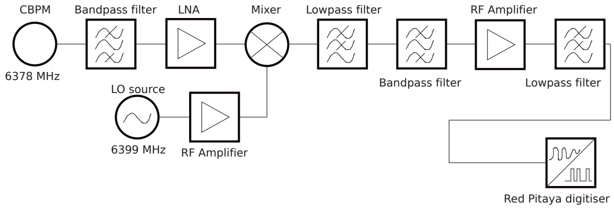

Figure 2: Schematic of the signal down-converting electronics for the C-band system.

In the first instance, we installed a single existing position cavity (Fig. 3) to commission the test system and start working on the electronics and DAQ, the data were taken on the 8th of July 2015.

We measured CBPM signals while moving the stages first in horizontal and then in vertical in order to measure the sensitivity of the cavity in hand. The digitised waveform signal was processed by the digital down-conversion (DDC) algorithm [6] on the host PC to detect the amplitude of the signal using a digital LO (Local Oscillator) of the same frequency as the incoming CBPM signal. A Gaussian filter was applied to remove the noise and up-converted component of the IF signal. For measuring the sensitivity of the cavity, the maximum amplitude of the demodulated signal

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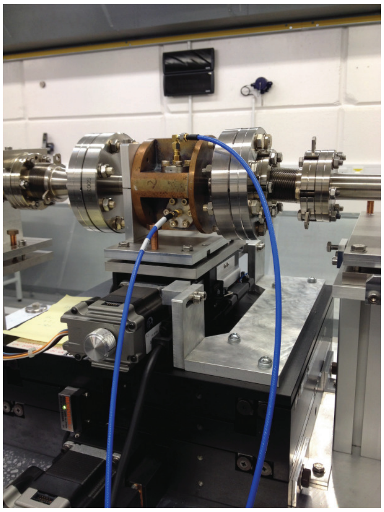

Figure 3: C-band BPM located on the VELA beam line. The CBPM is on the stepping motor which can move horizontally and vertically.

was sampled and propagated back to the cavity output using bench-measured conversion factors. Finally, the amplitude was normalised by the beam charge measured by VELA's wall current monitor. The measurement is shown in Fig. 4. We applied a fitting function $a|x-b|+c$ to the data, and the fitted position sensitivity (coefficient a of the fit) is consistent with the prediction of 1 mV/pC/mm calculated using the results of a 3D electromagnetic simulation with GdfidL [7].

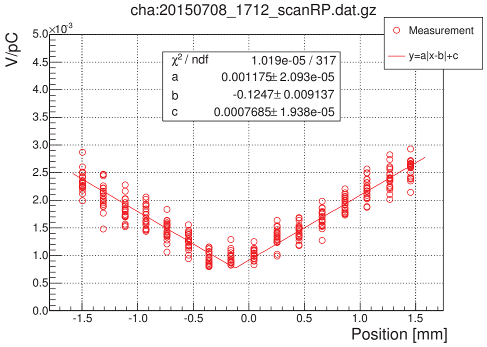

Figure 4: The normalised DDC amplitude vs. the CBPM horizontal position.

CURRENT DEVELOPMENTS

The CBPM hardware has been developed as following subsystems: position and reference cavities, signal processing electronics and DAQ system. Each subsystem is described in turn in the following sections.

Position and Reference Cavity Design

Both position and reference cavities are being developed. A reference cavity operates the monopole mode to provide the charge and phase normalisation of the offset signal, which otherwise depends on the charge and beam arrival time. The first prototype of the developed reference cavity is currently in the VELA beam line awaiting the next beam for testing (Fig. 5). A position cavity senses the beam offset via the dipole mode, which has a crest at the symmetry axis of the cavity and grows with the offset from it. The mechanical design of the position cavity is currently being finalised and is foreseen to be tested on a triplet of cavities in VELA beam line. The design draws on experience of manufacturing braze-free reference cavities. As a measure towards cost reduction, a thorough tolerance analysis has been carried out in simulation with the cavity dimensions varied in frequency and asymmetries introduced in cross-coupling studies.

Figure 5: Reference CBPM manufactured and assembled at FMB oxford.

Signal Down-Converter Electronics

The cavity signals are down-converted for digitisation. In this case, we deployed the classical heterodyne scheme, which is convenient for lowering the frequency of the signal close to the source for transmitting it to the digitisers outside of the accelerator enclosure, with the capability of high gain and efficient filtering at the intermediate frequency (IF), in this case 500 MHz. In the second stage of downconversion the frequency is lowered further to around 20 MHz, which is easy to convert with high bit resolution. The prototypes of the RF front-end and IF sections printed circuit boards (PCB) are shown in Figs. 6 and 7. They demonstrated the basic RF functionality in terms of the gain and noise characteristics as per cascaded system simulations. The next steps will include packaging these boards in a user-friendly format, where 2 possibilities are considered at the moment: standalone rack-mounted units with several channels per unit or single channel modules in a popular chassis format.

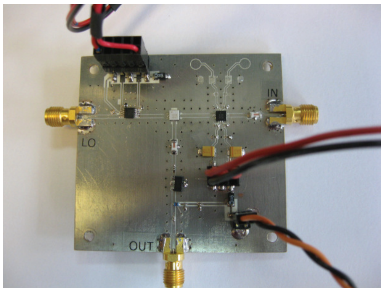

Figure 6: RF front-end PCB.

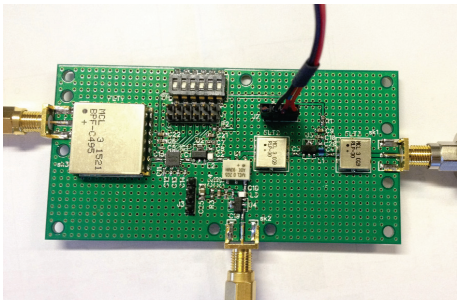

Figure 7: IF section PCB.

DAQ System

The baseline DAQ system is based on Red Pitaya boards, which are built around a SoC processor combined with an FPGA. Notably, the boards have 2 channels of 14 bit 125 MHz ADC, as well as 2 channels of DAC and GPIO lines. The sampling frequency and resolution are similar to that of a typical CBPM system, while GPIO lines can be used for control and monitoring. A faster version of the CBPM processing code may be implemented on FPGAs, in which case the DAC outputs can be used for generating feedback signals.

Insofar, EPICS channel access client API has been added to stock software as well as digital processing code for CBPM signals. Running processing on Red Pitaya is much more efficient with the external clock as many channels can be synced and the same phase reference used for all position channels. This requires minor hardware modifications, so an extension board is being developed for easy excess to the external clock and other features of the board (Fig. 8). Digital processing, currently running on the processor, will later be moved to FPGA part of the chip allowing for higher repetition rates.

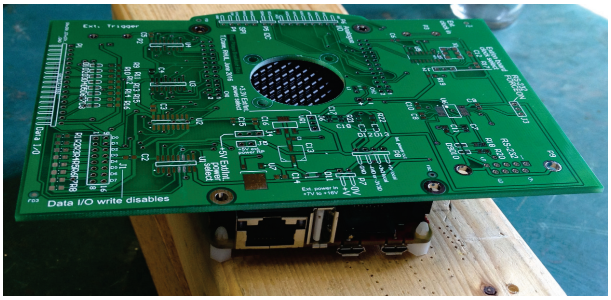

Figure 8: Extension PCB (unpopulated) on top of a Red Pitaya board.

Alternatively, the signal processing code can be executed on a centralised server, either on a rack controller hosting the digitisers or an external PC. This may be preferable when standard DAQ solutions exist locally.

CONCLUSION

The industrialisation of CBPMs has started, several subsystems have been tested, and a beam test prepared for position cavity prototypes. Most effort is now being put into manufacturing a test series of position cavities, with beam tests expected in 2017. Work on other subsystems will continue towards industrialising the developed designs into user-friendly robust systems. The whole system is expected to be tested at VELA and its performance characterised in various beam conditions.

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