MEASUREMENTS OF LONGITUDINAL COUPLED BUNCH INSTABILITIES AND STATUS OF NEW FEEDBACK SYSTEM

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Abstract

We have modified the vertical bunch-by-bunch feedback at Diamond Light Source to also provide a longitudinal kick on a separate input. Using our existing drive/damp system and a modulator/amplifier to the required 1.5 GHz we are thus able to characterise the damping rates of all coupled bunch instabilities, while not able to provide feedback. At the same time, we have started the development of a completely new longitudinal feedback system based on commercially available components, providing 500 MS/s, 14 bit conversion in and 16 bit out, powerful Virtex 7 field programmable gate array for digital signal processing and 2 GB of on board buffer for recording data. We report on the status of the development and our plans to bring the new system into use.

INTRODUCTION

At Diamond we have been working on *transverse* Bunch-by-Bunch Feedbacks (BBFB) for nearly a decade [1–4], and have concluded an major upgrade of the Digital Signal Processing (DSP) in firmware and software in 2014 [5–7] providing unique capabilities. So naturally, when asked to provide a *longitudinal* BBFB system to deal with potential Coupled Bunch Instabilities (CBI) introduced by Higher Order Modes (HOM) of a pair of normal conducting Radio Frequency (RF) cavities which will be installed at Diamond in summer 2017, we preferred to build one ourselves rather than opt for a commercial solution. However, our existing system is built around the *Libera Bunch-by-Bunch Processor* (LBBB) [8,9] which is unfortunately no longer available due to obsolescence of its components. Even if we had spares available in house, it did not appear prudent to build a new system based on 10 year old obsolete electronics, so we searched for an alternative.

After several discussions with potential suppliers we found the best option for us is to put together a system using modular commercially available Printed Circuit Board (PCB) components. We found this to be the better solution compared to having a dedicated PCB designed, as it avoids hardware development and the associated costs, and offers a path to a potential multitude of applications by re-using modular parts of the whole system.

At the same time, we thought what tests we could do before we would install the longitudinal kicker cavity, with its own lengthy development and manufacturing [10, 11]. We concluded that we could use a spare LBBB to provide drive signals and analysis of longitudinal CBI, which we would excite using the parasitic *longitudinal* coupling impedance of a pair of vertical kicker striplines driven in common mode (as opposed for the vertical kick which is achieved by driving the pair in differential mode).

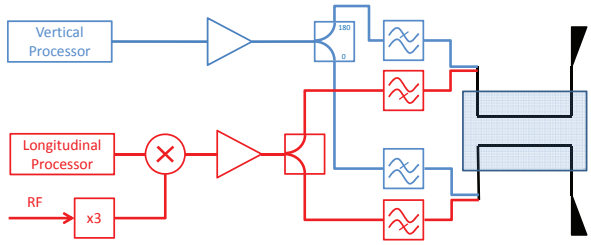

Figure 1: Block diagram of the connections of vertical and longitudinal BBFB to the vertical kicker stripline.

Consequently, the first part of the paper will concern the measurement setup and results for longitudinal CBI made so far using the vertical striplines, while the second part will summarise the status of our development of a new feedback processor.

LONGITUDINAL CBI MEASUREMENT

In search of providing longitudinal kicks with a bandwidth of 250 MHz without the dedicated longitudinal kicker installed, we found that the vertical striplines used as part of the transverse BBFB do provide a coupling as well. This coupling impedance scales with $\sin(\omega l/c)$ where l is length of the striplines (280 mm in our case) [12]. From this we select to excite the 250 MHz bandwidth below $3f_{RF} \approx 1.5$ GHz, which provides a strongly varying though always non-zero impedance.

The block diagram in Fig. 1 illustrates how we manage to continue to provide vertical BBFB while at the same time exciting longitudinal oscillations. The output for the vertical is amplified (at baseband 0-250 MHz) then fed through a 180° splitter to differentially drive the striplines. On the other side, the output for the longitudinal is up-converted to 1.5 GHz, then amplified and fed through a 0° power splitter to the striplines. Both signals are combined using a pair of diplexers with a cross over frequency of 1 GHz, thus allowing concurrent action in both planes.

We then apply a method of 'drive-damp' experiments described in more detail elsewhere [13] using a spare LBBB, with the only difference that on the longitudinal system we are driving at frequencies $\omega = (pM + \mu)\omega_0 + \omega_S$ with $p = 3$ (third RF harmonic), $M = 936$ our harmonic number, $\mu = 0, 1, \ldots, 935$ the scanned modes, ω_0 our revolution frequency and $\omega_S \approx 2\pi \cdot 2$ kHz our synchrotron frequency.

Part of the analysis of CBI is already done in the FPGA as part of our DSP code implemented in the LBBB [6]. We are measuring the complex amplitude of the driven mode

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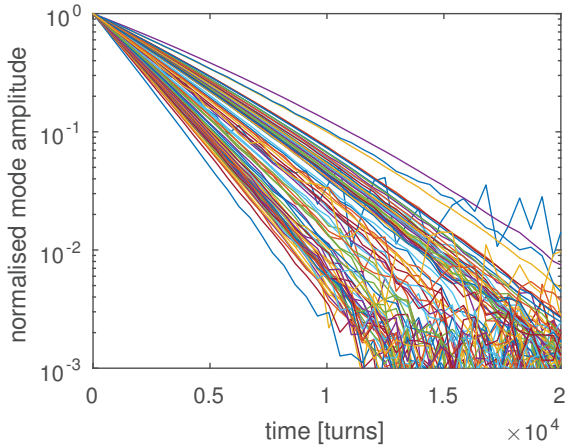

Figure 2: Normalised magnitude during damping of longitudinal CBI after excitation. Only every tenth mode of the total of 936 is shown for clarity.

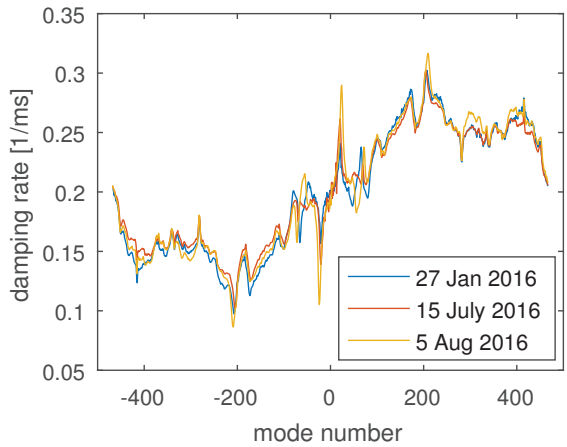

Figure 3: Damping rates of all longitudinal CBI.

by multiplying the input bunch position stream with $\sin(\omega)$ and $\cos(\omega)$ and averaging the result over two synchrotron periods (480 turns). We then only record this complex amplitude for 10 points during the drive time (4800 turns) and 50 points (24000 turns) during the damping (when excitation is switched off and natural damping is observed). The FPGA then immediately advances to the excitation of the next mode, scanning through 18.5 modes every second and completing a whole set of 936 grow damp experiments in 52 s.

The advantage of this upstream FPGA processing is a massive reduction of the data that needs to be transferred out: in 52 s the ADC has produced $52\,\text{s} \cdot 500\,\text{MHz} \cdot 2\,\text{B} \approx 48.4\,\text{GB}$ of data, while our on-board analysis reduces this to a mere $60 \cdot 936 \cdot 4\,\text{B} \approx 219\,\text{kB}$.

Measurement Results

In order to improve further on the signal to noise ratio, we repeat the whole 936 mode grow-damp experiment 100 times and compute the average complex amplitudes of that. The magnitude of a subset of mode amplitudes during damping is shown in Fig. 2. By fitting the natural logarithm of the mode amplitudes with straight lines, we directly retrieve the damping rates.

These damping rates have been measured three times during operation with 300 mA stored beam and are shown in Fig. 3. The average damping rate of $0.2\,\text{ms}^{-1}$ is synchrotron damping, while the deviations are caused by the aliased impedance of the whole machine. The overall pattern is nicely symmetric around mode 0 as is predicted by theory. The most critical point is then mode -209 which has the lowest damping rate, so this mode would go unstable first if beam current was increased to 550 mA or earlier if damping was reduced for instance by powering off one or both of the two super conducting wigglers.

The sharp resonance at mode -10 is also interesting as it has changed over the course of these three measurements. Potentially, this could be related to a HOM of our RF cavities moving slightly during this time. We plan further investigations of this for instance with one cavity parked.

NEW FEEDBACK PROCESSOR

The demands on a feedback processor are quite clearly defined: its interfaces are analogue signals in and out which range from DC to half bunching frequency, typically pre-processed by a low level RF front-end and post-processed by a modulator including potential frequency translation. Analogue to Digital (ADC) and Digital to Analogue Converters (DAC) sampling at precisely the bunching frequency will connect to a Field Programmable Gate Array (FPGA) in which DSP routines are used to provide the actual feedback and additional functionality. Latency through the whole system needs to be fully deterministic down to the few 10 ps level, and group delay needs to be flat to the same level over the whole range of operation from DC to half bunching frequency.

Hardware

We found an FPGA Mezzanine Card suitable for this specification in the *FMC-500* [14], which offers two channels of ADC at up to 500 MS/s, 14 bit and two channels of DAC at up to 1230 MS/s, 16 bit. A flexible on board Phase Locked Loop (PLL) chip allows for synchronisation of the conversions with an externally delivered RF clock. A framework for FPGA support is available, however as this is designed for Innovative Integration FPGA boards only we found little use of it. So we resorted to writing Serial Peripheral Interface (SPI) and drivers to set up the integrated circuits and routed the data channels to the FPGA.

This FMC module needs to be connected to a carrier with an FPGA, and to this end we selected the *AMC525* [15], which features a Virtex 7 690T, 2 GB of on board Double Data Rate 3 (DDR3) memory, 2 High Pin Count (HPC) FMC slots, Peripheral Component Interconnect Express (PCIe) and Gigabit Ethernet connections on the rear connector and an on board Freescale QorIQ PPC2040 processor

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Figure 4: Photo of the assembly of FMC-500 (top right) and FMC-DIO-5Ch-TTL-A (bottom right) on the AMC525. Dimensions are 180 mm by 150 mm.

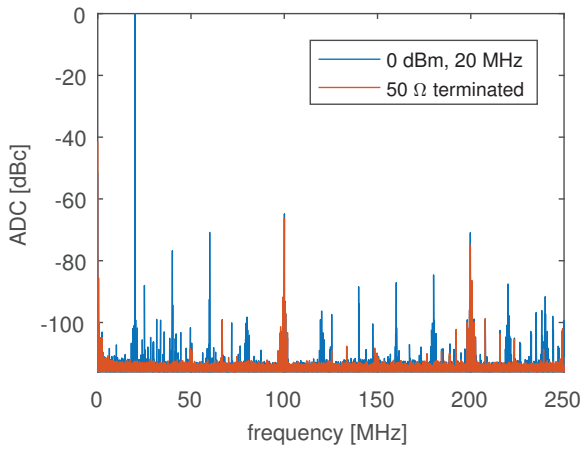

Figure 5: Spectrum with and without a 0 dBm 20 MHz tone (filtered by a crystal to remove harmonics from the generator). Fast Fourier Transform of 2^{25} points.

for FPGA firmware uploads from a 32 GB flash memory. The processing capabilities of this FPGA are by far superior to the LBBB, for instance it offers 3600 DSP blocks where the Virtex 2 provided only 136.

In the other FMC slot on the *AMC525* we place a *FMC-DIO-5Ch-TTL-A* Open Hardware Module [16], which we use for additional trigger signals. Again, the FPGA interface to this had to be developed by us, but integration turned out to be straight forward.

Finally, the stack of two FMC modules on the carrier (as shown in Fig. 4) is used inside a *VT814* Micro-TCA crate which also houses a Intel processor card *AMC720* [15] which runs our standard install of Redhat Enterprise Linux on which we will implement an EPICS driver. For this selection we were motivated by alignment with other use cases to select a rather larger crate with redundant power supplies.

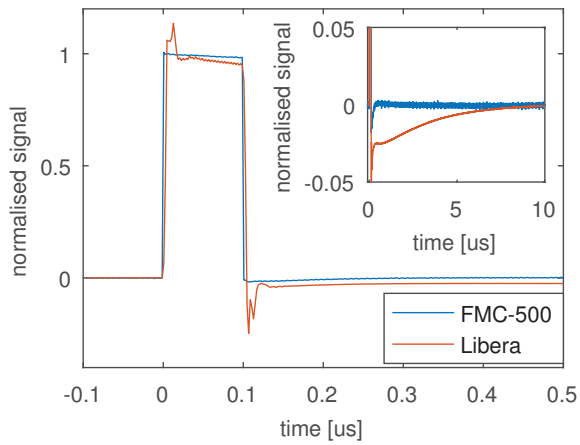

Figure 6: Normalised time response to a 100 ns pulse. Main graph shows pulse detail, while inset shows longer term settling.

Programming

We have implemented the following on the FPGA so far: a Peripheral Component Interconnect Express (PCIe) interface to the Central Processing Unit (CPU), two DDR3 memory controllers, an 256 bit wide Advanced eXtensible Interface bus to transport data between these and the ADC, DAC and our DSP application as well as register interface and SPI to configure ADC, DAC and PLL on the FMC-500. We also implemented a low-voltage differential signaling parallel interface for the ADC and DAC data flows with associated clocks.

PCIe and SPI are supported on the CPU with Linux drivers and utilities also developed in house. We have convinced ourselves that reading the memory on the *AMC525* works reliably and at swift speeds of 2 GB/s. Copying this into CPU memory slows the process to 1 GB/s, while subsequent reading and converting to double length floating point numbers in Matlab® is managed at 290 MB/s, which is still more than 100 times faster than the comparable procedure on the LBBB.

For producing a good sample clock from the externally supplied bunching frequency f_{RF} we have two options: Either we feed it straight through the PLL circuit, or we configure the PLL circuit to lock its voltage controlled oscillator at $5 f_{RF}$ to the external input and then output 1/5 of that frequency as sample clock. We have evaluated both options, and the straight through option delivers better phase noise at small offset frequencies of 1-10 kHz, which is particularly important for longitudinal feedbacks which look for synchrotron oscillation sidebands just a few kHz away from harmonics of the revolution frequency.

Finally, we have begun operating the ADC to the DDR3 and subsequently reading out the memory into Matlab® (running on the *AMC720*). This way we have managed to provide evidence of the excellent dynamic range (see Fig. 5). It shows that the 3rd harmonic at -70 dBc is the

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highest harmonic (and that might still come from the generator despite the crystal filter used), while there are signals visible around 100 MHz and 200 MHz even without input signal originating from the reference clock (fundamental and higher harmonics aliased back). We are investigating if this unused device can be switched off or removed.

The impulse response of this DC coupled ADC compared to the AC coupled LBBB (see Fig. 6) is also excellent. While the splitting of the input into four 125 MS/s samplers on the LBBB lead to some few ns long spikes and the AC coupling lead to drooping of the flat high and low signals, both these effects are absent on the *FMC-500*.

CONCLUSIONS

We presented measurements of longitudinal CBI in the current state of the Diamond storage ring before installation of normal conducting RF cavities. We plan to continue using this system for comparative measurement beyond the installation of the dedicated longitudinal kicker cavity in March 2017 and up to the installation of the normal conducting RF cavities in Summer 2017.

At the same time we will continue to finish the implementation of the new BBFB by adding our DSP code and EPICS driver. The complete system will provide a capable system not only for our longitudinal BBFB, but can also be used without modification for the transverse. We hope that by selecting commercially available modular components there will be interest in this system also at other accelerators.

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