A PPS COMPLIANT INJECTED CHARGE MONITOR AT NSLS-II*

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Abstract

The Accumulated Charge Monitor Interlock (ACMI), a PPS compliant system, was developed to ensure the Accelerator Safety Envelop (ASE) limits for charge generation in the NSLS-II Injector are never violated. The ACMI measures the amount of charge in each injection cycle using an Integrating Current Transformer (ICT). For logistical reasons, adding a redundant ICT was impractical so in order to achieve the high reliability required for PPS this system is designed to perform self-tests by injecting calibrated charge pulses into a test coil on the ICT and analyzing the returning charge signal. The injector trigger rate is 1.97Hz and self-tests are performed 250 msec after every trigger pulse. Despite the lack of a redundant charge measurement the ACMI achieved the high reliability rating required for PPS with a mean time between failure (MTBF) rate greater than 10^6 hours. The ACMI was commissioned in 2014 and has operated to date without any major problems. In 2015 a second ACMI system was commissioned to monitor charge in another region of the injector system.

INTRODUCTION

The ASE sets limits on the maximum charge allowed in a single injection shot and the maximum accumulated charge allowed in a one-hour window. The ASE also sets a limit on the one-minute accumulated charge during Top-Off operations at the NSLS-II facility. The ACMI was developed as part of the NSLS-II PPS to ensure that these ASE limits are never violated. The ACMI uses a single ICT to make the charge measurement. It was not practical to install a second ICT which would have allowed redundant charge measurements to be made. Complicating matters further, the ICT (Bergoz ICT-CF6"-60.4-40-70-20:1) is not a safety-rated device and the ACMI must assume that it can fail at any time. Without a redundant measurement the ACMI would have to use a different strategy to ensure that the single charge measurement is accurate. The ICT came equipped with a test coil which is used by the ACMI to perform self-tests between each injector trigger. For each self-test the ACMI launches a calibrated charge pulse to the ICT test coil and analyzes the returning charge signal in the same manner as the actual beam. Any deviation between the expected and measured charge values for the self-tests generates a fault. The LINAC trigger signal is not generated by a PPS compliant system and the ACMI must assume that the trigger signal could fail at any time. The ACMI carefully monitors the trigger timing applying strict limits on the trigger rate. The ACMI also monitors the ICT at all times ensuring that charge is only detected within a proper time window derived from the trigger timing. The ACMI was required to undergo independent reliability analyses and rigorous internal reviews to ensure the system is PPS compliant.

ACMI SYSTEM

Figure 1 shows the block diagram for the ACMI. The system is built around a safety-rated PLC (Fig. 2: Allen-Bradley 1768-43S). Two PCBs were designed for this system, the Timing Generator and the Analog Processor. An HMI panel allows diagnostic information to be displayed on the ACMI cabinet. The PLC also sends diagnostic information to an EPICS IOC for remote monitoring and data archiving. A few analog and critical timing signals are sent to a VME digitizer for further monitoring. Any fault detected by the ACMI disables the LINAC gun. The only user inputs into the ACMI are PPS compliant reset signals to clear any latched faults.

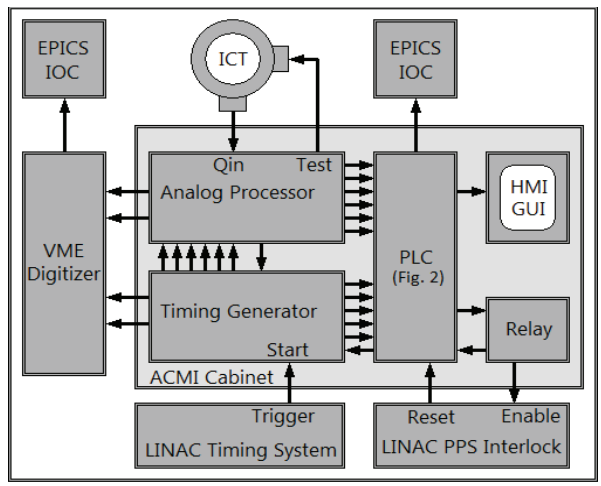

Figure 1: ACMI block diagram.

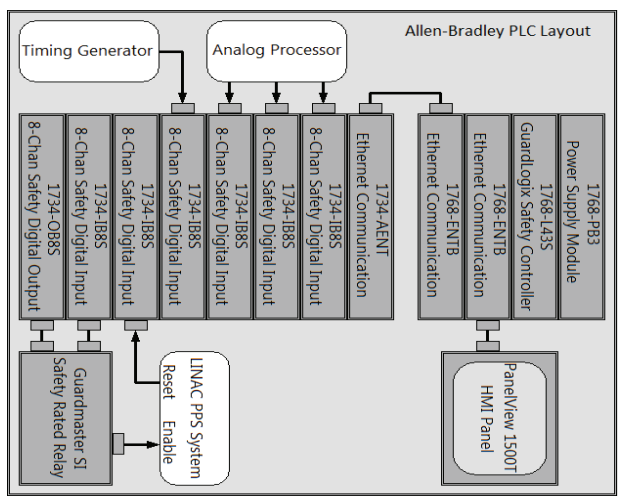

Figure 2: PLC layout.

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Timing Generator

A block diagram for the Timing Generator is shown in Fig. 3. The system is designed around an Altera Complex Programmable Logic Device (CPLD) (EPM3128A) which is clocked by a 100 MHz oscillator. The CPLD is programmed using Quartus-II software and an algorithm was developed to generate all the critical timing signals required to process the charge signals for the beam and for the self-tests. A trigger signal from the LINAC timing system initiates the timing sequence. Figure 4 shows the basic timing signals generated to process the beam charge signals on the Analog Processor. Processing of the beam charge is completed in under 100 usec. 250 msec after the LINAC trigger the Timing Generator initiates a self-test by creating a Test pulse that is reshaped on the Analog Processor and driven into the ICT test coil. The timing sequence shown in Fig. 4 is repeated for the charge signal generated by the self-test. Processing of the self-test is completed before the arrival of the next trigger signal.

The trigger signal is not PPS compliant and therefore must be monitored carefully. The Timing Generator measures the time delay between each trigger pulse and will generate a fault if the 1.97Hz trigger frequency appears to change by more than +/-2%. If the Analog Processor detects a charge signal above a threshold setting then a charge-above-threshold signal (QAT) is sent to the Timing Generator. The Timing Generator issues a fault if the QAT signal falls outside the proper integration window (SampA in Fig. 3) indicating that charge was detected at a time it was not expected.

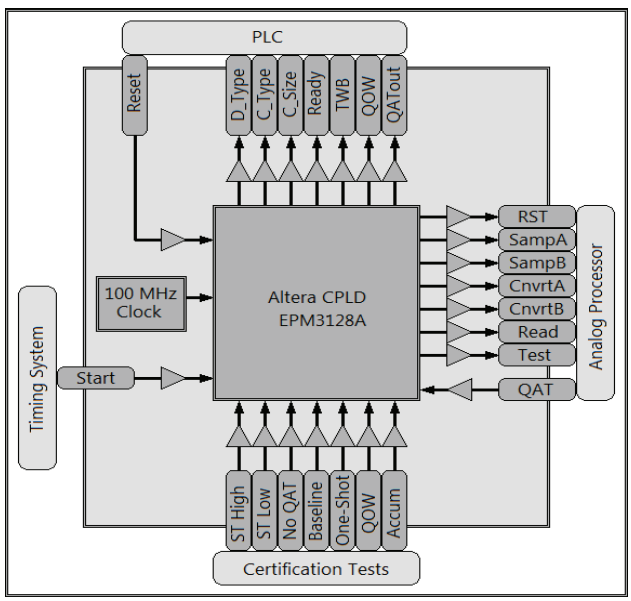

Figure 3: Timing generator block diagram.

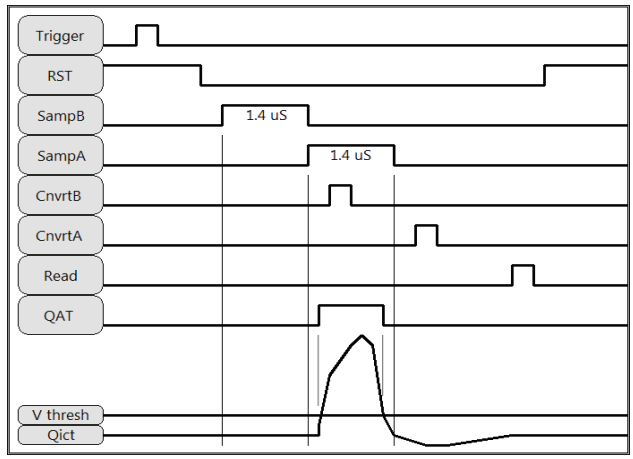

Figure 4: Basic timing diagram.

A series of inputs into the Timing Generator are provided which allow operators to generate various fault conditions on demand. This is useful during annual ACMI re-certifications where detection of every fault mode is tested and verified.

Analog Processor

A block diagram of the Analog Processor is shown in Fig. 5.

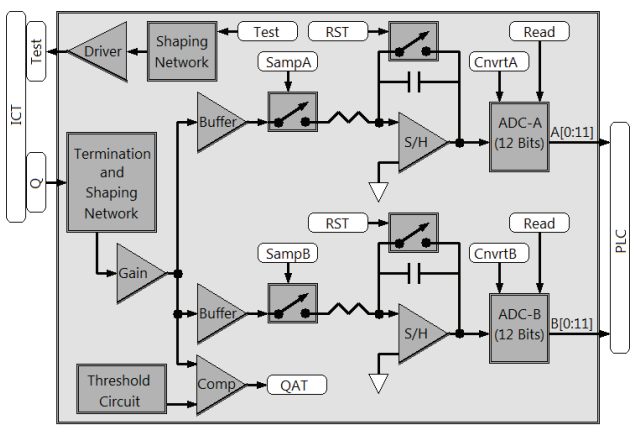

Figure 5: Analog processor diagram.

The charge signal from the ICT passes through a termination and shaping circuit in order to increase its size and width before integration. This signal is passed to two identical sample-and-hold (S/H) amplifiers. Critical timing signals (shown in Fig. 4) are used to perform the integration of the amplified charge signal and the baseline signal which immediately precedes the charge signal. Once integration is complete the value is held on the S/H amplifiers until they are digitized on two ADCs using other timing signals. When digitization is complete the data is sent to the PLC for further processing.

Another copy of the amplified charge signal is also sent to a comparator where it is compared to a threshold voltage. The threshold voltage is set as low as possible to detect very small charge signals but high enough so that it

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is above local noise sources. At NSLS-II this threshold is set low enough to detect injected shots as small as 0.15nC. The comparator output generates the QAT signal that is used in the Timing Generator to determine if the detected charge falls within the proper time window.

For each self-test, a Test pulse from the Timing Generator is reshaped on the Analog Processor and driven into the ICT test coil. The Timing Generator produces all the critical timing signals so that the returning charge signal for the self-test can be processed on the Analog Processor in the same manner as the actual beam.

Reliability Studies

Since the Timing Generator and the Analog Processor were new designs they were required to have an independent reliability analysis. A fault-tree analysis and a thermal stress analysis were performed on each design[1]. The fault-tree analysis uses reliability data for each component on the PBC to determine the probability of failure for every critical signal path in the design. The thermal stress analysis determines the probability of failure based on the heat load calculated for each component. In both cases the MTBF rate was determined to be well above the required 10^6 hours. These designs were also extensively reviewed by engineering and safety experts at NSLS-II who approved their use in the NSLS-II PPS.

PLC Processing

The PLC processes the beam data by first subtracting the baseline measurement from the charge measurement to obtain the charge reading. There are two FIFO stacks in the PLC where charge is accumulated. The larger stack contains all charge readings for the past hour (about 7092 entries) and the sum of all these readings is compared to the one hour ASE limit. The smaller stack contains all charge readings over the past minute. The smaller stack accumulates readings only during Top-Off operations at NSLS-II and the charge sum is compared to the one minute ASE limit. While processing each beam event the PLC monitors for all fault conditions listed in Table 1:

Table 1: Beam Generated Faults

Fault Condition	Limit
Charge Reading HIGH	>16.0nC
Charge Reading LOW	<-0.2nC
Baseline Measurement HIGH	>0.2nC
Baseline Measurement LOW	<-0.2nC
LINAC Trigger Rate HIGH	>2.1Hz
LINAC Trigger Rate LOW	<1.9Hz
1-Hour Accumulation Rate HIGH	>82.9uC/Hr
1-Min Accumulation Rate HIGH	>30.0nC/Min

The self-test are processed in the PLC in much the same way as the beam however the self-test readings are not accumulated. The timing for the beam is set up so that on the Analog Processor ADC-A digitizes the charge signal and ADC-B digitizes the baseline. The charge reading for the beam is obtained by performing an (A-B) subtraction. Half of all self-tests use this (A-B) timing scheme and the other half use a (B-A) timing scheme where the roles of the two ADCs are reversed. The two timing schemes are used to verify that both digitization paths through the Analog Processor are working correctly. Self-tests also occur in two sizes, 17nC and 0.5nC which span the range of injected shots typically produced at NSLS-II. Since both sizes for self-tests are above the 0.15nC charge threshold every self-test must generate a QAT signal. The two timing schemes and the two sizes result in four different self-tests. One self-test is performed after each LINAC trigger and all four self-test will be performed for every four LINAC triggers. The Timing Generator tells the PLC which self-test is being performed. While processing self-tests the PLC monitors for all fault conditions listed in Table 2:

Table 2: Self-Test Generated Faults

Fault Condition*	Limit
17nC Self-Test HIGH	>17.5nC
17nC Self-Test LOW	<16.5nC
17nC Self-Test Baseline HIGH	>0.2nC
17nC Self-Test Baseline LOW	<-0.2nC
0.5nC Self-Test HIGH	>0.53nC
0.5nC Self-Test LOW	<0.47nC
0.5C Self-Test Baseline HIGH	>0.2nC
0.5nC Self-Test Baseline LOW	>-0.2nC
17nC Self-Test with no QAT	N/A
0.5nC Self-Test with no QAT	N/A

*For both (A-B) and (B-A) timing schemes

The PLC also monitors itself and will issue a fault if any of its internal watchdog timers are violated or if communication to any of its IO modules is interrupted.

Noise Considerations

Whenever a charge signal is above the 0.15nC threshold a QAT pulse is generated. The Timing Generator determines if the QAT pulse lies within the integration window for the beam or self-test. If the QAT pulse is outside the integration window then a charge-outside-window (QOW) fault is issued. QOW events cannot be accumulated and might result in an ASE limit violation so it is vital that they are all detected. Noise sources present a challenge if they cross the 0.15nC threshold. If a large noise spike generates a QAT signal it will almost certainly lie outside the integration window and the ACMI will declare a QOW fault. These events form the majority of nuisance trips generated by the ACMI and are usually due to operations of nearby klystrons or pulsed magnet systems. Transients from these systems get picked up along the coaxial cables run between the ICT and the ACMI. Charge signals generated by the ICT propagate along the cables as a balance current signal while transient noise propagate as an unbalanced signal. Passing the coaxial cable through ferrite beads will attenuate any unbalance signal while leaving the balanced signals unaffected. With properly

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chosen ferrite beads it was possible to reduce the size of the transient signals by more than 30dB. Careful routing of these cables away from noise sources and the use of grounded conduits further reduced the size of the transient noise. By the time the ACMI was commissioned the rate of nuisance trips was reduced to acceptable levels.

It was also important to use high-quality linear power supplies with the ACMI and to have a carefully planned grounding scheme eliminating ground loops. Many different isolation techniques (optoisolators, pulse transformers, etc) were employed in the ACMI especially on the Analog Processor where the high precision measurement is made. Applying all these techniques, the ACMI achieved a level of accuracy equal to a Bergoz NPCT module with a full-scale accuracy of 0.1%.

ACMI Calibration, Certification and Operation

As part of the NSLS-II PPS the ACMI must undergo an annual calibration and certification procedure [2,3]. The first part of the calibration procedure determines the signal ratio between the test input and the charge output of the ICT. These measurements are made with calibrated bench equipment and not the ACMI. The ratio measurement is performed primarily to determine if the ICT properties are changing due to aging effects. The second part of the calibration procedure involves sending charge pulses of varying sizes between 0.5 and 19nC to the test coil of the ICT and comparing the ACMI reading to the reading obtained using the bench equipment. The calibration constants for the ACMI are determined from this data.

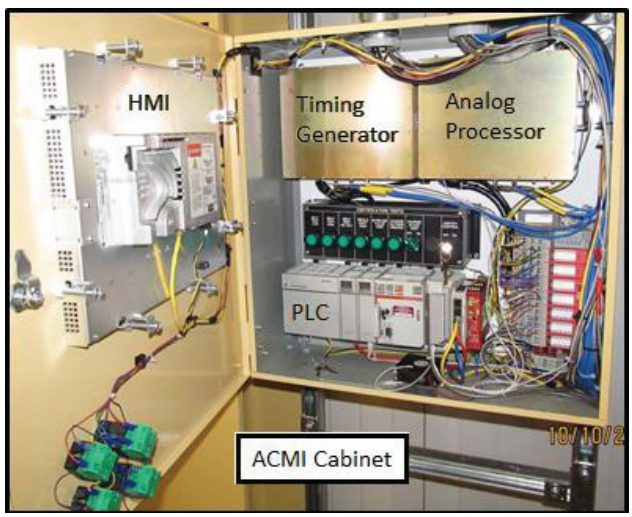

Figure 6: ACMI cabinet.

The certification procedure requires a demonstration that every fault mode described earlier be correctly detected and processed by the ACMI. It is not permitted to use actual beam for these fault tests. The Timing Generator is used to generate many of the fault conditions. Within the ACMI cabinet (Fig. 6) a panel is provided to generate most of the system faults (Fig. 7). Pressing any of these buttons will cause the Timing Generator to produce test pulses that mimic the conditions for that fault. The test pulses are sent to the ICT test coil and the returning charge signal is processed by the ACMI in the normal manner. The ACMI must detect the indicated fault to pass that test. There are also procedures to generate any fault not covered by this panel.

Once the calibration and certification procedures are complete the ACMI can be put into operations for up to one year. While in operations the ACMI is constantly monitored for any condition that might affect its performance. Diagnostic information for the ACMI is presented at the ACMI cabinet on an HMI monitor and remotely using an EPICS based GUI. All ACMI readings for both the actual beam as well as the self-tests are archived. Archived data is analyzed off-line to determine if there are any disturbing trends.

Figure 7: Certification test panel.

Conclusion

Charge monitoring systems for injector systems have been around a long time but are generally not safety-rated systems. The need to integrate these systems into the PPS has become an important issue for any modern facility. Meeting the requirement for PPS can be very difficult and the ACMI faced many problems:

- No redundant measurement
- Incorporation of non-safety-rated devices
- Incorporation of newly designed devices
- High noise levels from external systems
- Exhaustive review process

The ACMI overcame all these obstacles and in 2014 this system was fully integrated into the NSLS-II PPS. In 2015 a second ACMI system was commissioned to monitor charge in a different part of the injection system.

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