DIAGNOSTIC DATA ACQUISITION STRATEGIES AT FRIB *

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Abstract

Strategies for data acquisition and processing will be discussed in the context of the Facility for Rare Isotope Beams (FRIB). Design decisions include selecting and designing electronics hardware, data acquisition cards, firmware design, and how to integrate with EPICS control system. With over 300 diagnostic devices and 16 unique types of devices, timing for synchronous data acquisition is important. Strategies to accelerate development as well as reduce maintenance requirements will be discussed, including using common hardware and firmware whenever possible, and defining a common data reporting structure for use by most devices. MicroTCA.4 platform is used to integrate data acquisition cards, distribute timing information, and machine protection signals.

FRIB MACHINE REQUIREMENTS

The Facility for Rare Isotope Beams (FRIB) is a new scientific user facility for low energy nuclear science. Under construction on campus and operated by Michigan State University, FRIB will provide intense beams of rare isotopes [1].

FRIB will deliver the highest intensity beams of rare isotopes available anywhere. The superconducting linear accelerator (linac) will accelerate ion species from ¹⁸Ar up to ²³⁸U with energies of no less than 200 MeV/u and provide beam power up to 400 kW. Although designed to support full-scale CW operation, low current and pulsed modes will also be utilized, so diagnostics must support a large dynamic range, from 1 nA to 1 mA of beam current. Figure 1 shows a schematic overview of the accelerator.

Machine Protection and Availability

In order to achieve high reliability and high availability, permanent accelerator component damage should be prevented, beam loss and residual activations should be minimized, and beam downtime minimized. This leads to an array of diagnostic devices which monitor a variety of beam loss mechanisms. A machine protection system (MPS) has been designed to detect and respond quickly (< 35μ sec) to beam loss events and terminate the beam [3]. This is achieved by monitoring not-OK (NOK) signals from a multitude of MPS nodes which digitize diagnostic data and make local NOK decision in less than 15 µsec. The remaining 20 µsec of the time budget is used to communicate the NOK signal to the MPS Master and to terminate beam production and transport. Table 1 is simplified picture of the acute (fast) and chronic (slow) losses which we must detect. Table 2 shows an overview of diagnostic devices utilized not only for machine protection (MPS), but * This material is based upon work supported by the U.S. Department of Energy Office of Science under Cooperative Agreement DE-SC0000661, the State of Michigan and Michigan State University. † cogan@frib.msu.edu

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and

also for tuning, commissioning, and general diagnostic information [2]. Italicized devices * will provide input to MPS.

Table 1. Acute and Chronic Deam Loss Detection	Table	1: Acute	and	Chronic	Beam	Loss	Detection
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Beam Loss	Diagnostic Response Time
100% (2 J)	15 usec
10% (0.2 J)	150 usec
Slow (0.1 W/m)	seconds

Table 2: FRIB Diagnostic Devices

Device	Total #
Beam Position Monitor *	149
Beam Current Monitor (ACCT) *	12
BLM - Halo Monitor Ring *	66
BLM - Ion Chamber *	47
BLM - Neutron Detector *	24
BLM – Fast Thermometry System *	240
Profile Monitor (Lg., Sm. Flapper)	41
Bunch Shape Monitor	1
Allison Emittance Scanner (2 axis)	2
Pepper pot emittance meter	1
Wire Slit Emittance Scanner (2 axis)	1
Faraday Cup	7
Fast Faraday Cup	2
Viewer Plate	5
Selecting Slits System - 300 W	5
Collimating Apertures - 100 W	2
Intensity Reducing Screen System	2

Implications for Data Acquisition

To achieve MPS requirements (not all of which are discussed here, see [3]), diagnostic devices should have a response time of 5 µsec (analog bandwidth DC to 35 kHz), digitized sample rates of at least 1 MS/sec and support a large dynamic range, from < 1 nA to 1mA, depending on the device. To respond to beam loss events in less than 15 usec, MPS decisions are made in real-time locally by the data acquisition electronics. Field programmable gate arrays (FPGAs) are utilized to provide real-time signal processing and MPS decision, with close integration to digitizing hardware, often combined in a single electronics board. Additionally, FPGAs allow custom firmware to incorporate accurate timestamp from a global timing system (GTS) and provide ability for improved signal processing, including digital filters, background noise subtraction, advanced threshold triggering, etc.



Figure 1: Schematic of FRIB accelerator, three linac segments and two folding segments.

Beam Modes and Structure

Figure 2 illustrates various beam modes at FRIB. The primary beam mode will deliver near continuous (CW) beam, however, a 50 usec beam gap is introduced at ~100 Hz to reset beam current transformer readings and facilitate sampling of signal backgrounds. This leads to actual duty factor of 99.5%. Pulsed modes are used to achieve relatively low duty factor for beam commissioning and tuning. Beam power ramp-up modes exist to slowly heat the isotope production target and avoid damage to due to thermal shock. The duty factor ramps from 0% to 99.5%, with up to 250 beam on / off pulses during each 10 msec cycle. The beam structure for each 10 msec cycle is broadcast to the data acquisition hardware by the global timing system (GTS), which indicates beam events such as start-of-cycle (every 10 msec), beam on / off, and global timestamp events. The 50 usec beam gap for diagnostics appears at the beginning of every 10 ms beam cycle, so the processing of background signal continues regardless of beam mode (pulsed, CW, or ramp-up). Modulation of the CW beam current is performed with an electrostatic chopper in the Front End, upstream of Linac Segment 1.

Global Timing System

The global timing system (GTS) distributes event codes across the system to keep all receivers aware of the state of the beam (on or off), start-of-cycle events (with or without beam), global timestamp (POSIX time), and custom diagnostics codes for synchronized trigger acquisitions. GTS event codes are distributed by fiber optic throughout the machine, providing up to 1 event code every 80.5MHz, which is locked with the fundamental RF cavity frequency. Each data acquisition (DAQ) device connected with MPS needs access to this information to keep local data timestamps in sync with global clock, and to respond appropriately to various beam modes.

DATA ACQUISITION HARDWARE

At FRIB there are hundreds of diagnostic devices requiring connections to both MPS and GTS systems, in addition to network connections to the control systems network, EP-ICS. A potentially large number of fiber optic (GTS), Ethernet (EPICS), and trigger signal (MPS) cables need to be managed.

In addition to these connectivity requirements, the variety of diagnostics devices have different requirements and operating modes. Some are continuously monitoring,



Figure 2: Illustration examples of beam modes and timing, (a) continuous CW mode, (b) pulsed beam mode, and (c) ramp-up beam mode.

while others are intermittent-use. Some have MPS requirements, others do not. Diagnostic devices have varied response times and dynamic range requirements.

It is an option to design a unique data acquisition (DAQ) system for each device, with connections and components optimized for each device. However, a large number of unique DAQ systems can ultimately be quite burdensome to develop and maintain.

Simplification: Leverage Commonality

Leveraging hardware commonality has been a design goal for the FRIB diagnostics DAQ systems. It should be clear that utilizing a small number of DAQ systems results in fewer systems to learn, develop, and maintain. In the short term, the full diagnostic scope can be developed more rapidly. Much of the firmware and software interfaces can be shared, for faster development and passing new feature updates to multiple devices. In some cases, we also adapted electronics designed in-house or open source for our diagnostic applications, with minor changes. Some of the efforts to simplify hardware, firmware, and software will be discussed in detail.

MicroTCA Chassis-Based Platform

A chassis-based hardware platform has significant advantages for FRIB diagnostics. While individual "pizza box" systems were considered for some systems, a chassis platform with multiple payload slots demonstrated several advantages. Advantages include common power supply management, thermal management, easy to add/replace boards, and common data busses between cards in the chassis for shared signals, reducing need for external cables.

While many card carrier platforms exist, it was desired to avoid those which were proprietary, which tend to be expensive and sometimes difficult to integrate with custom hardware. VME and MicroTCA.4 [4] [5] were two relatively open standards which were considered, both of which see significant usage at physics research installations. A thorough comparison of these technologies is beyond the scope of this paper, but MicroTCA.4 was chosen as the primary platform for our fast-sampling diagnostics with connection to MPS. MicroTCA's use of modern highspeed serial busses such as PCIe (Gen3) and Ethernet (GbE) provide fast access to data, allowing us to consolidate numerous EPICS drivers (IOC) into a single CPU module, one per chassis. VME and CompactPCI primarily support slower legacy parallel busses. MicroTCA also includes some valuable features such as remote power module management, thermal management and monitoring, and support for rear-transition-modules (RTM) which provide additional input/output interface.

MicroTCA is a more complicated standard than some alternatives, and we experienced significant compatibility issues early on, most of which have been addressed. With most issues resolved, we have managed to build some robust and reliable test systems. MicroTCA allows us to leverage several commercial off-the-shelf (COTS) modules, such as the chassis, power module, processor card (CPU), and MicroTCA Carrier Hub (MCH). For MicroTCA DAQ cards, many COTS and customized COTS options exist.

MicroTCA Backplane Signals

MicroTCA has allowed us to significantly simplify the cabling to various control systems. The AMC backplane provides power to each card, as well as data busses between cards, such as PCIe, Ethernet, and general use M-LVDS I/O ports. While each chassis can contain up to 12

payload DAQ cards, for diagnostics we use two slots to consolidate key interfaces to the larger control system, using the AMC backplane for intra-chassis distribution, illustrated in Fig. 3.



Figure 3: MicroTCA data bus distribution.

The first slot is a processor card (CPU) which is the single interface to the EPICS control system network, with multiple IOC drivers running on Debian Linux OS. MicroTCA backplane provides switched PCIe connection to each DAQ card, and measurement and configuration data is passed simply between CPU and DAQ cards by PCIe register reads and writes. An Ethernet protocol stack is not necessary in the FPGA, and is completely handled by Linux running on the CPU module.

The second slot is for our event receiver (EVR). This is a custom FPGA-based board which receives and decodes events from the GTS fiber bitstream and handles the interface to the MPS system, utilizing custom trigger in/out signals. The GTS and MPS signals utilize bidirectional M-LVDS signals on the AMC backplane, part of the MicroTCA standard generally utilized for passing triggers and interlocks (ports 17-20). The GTS and MPS signals are distributed in parallel to all other cards in the chassis, while the EVR card monitors and consolidates the MPS not-OK (NOK) signals from each card.

The end result is a MicroTCA chassis with up to 10 DAQ cards, one fiber optic interface to GTS, one interface to MPS, and one Ethernet drop, capable of monitoring up to 80 or more channels / devices.

Data Acquisition (DAQ) Hardware

We utilize FGPAs and custom signal processing algorithms to meet our real-time MPS requirements, but developing custom firmware for FPGAs is often challenging and time-intensive. We would like to share hardware and firmware between as many diagnostic devices as we can.

Since leveraging common hardware for different devices can often lead to common/shared firmware development which can lead to common software drivers and software modules, it is clear that hardware choices have a ripple effect that can significantly impact the scope of work for software and application developers downstream.

DAQ hardware that meets the strictest requirement can often be utilized for devices with an easier requirement. In that case, the DAQ hardware may be over-specified and more expensive than a lower cost alternative, but the benefits for shared development and sourcing may outweigh the potential upfront material costs. For example, a DAQ card with a time response of 5 μ sec can serve a device with a longer time response. A sample rate of 1 MS/sec may not be required for every device, but it is straightforward to integrate and decimate to lower sample rates.

FRIB device requirements were collected and analyzed, and plans were made to consolidate these to a small number of DAQ boards. Firmware was also designed to offer runtime configurability for certain aspects related to MPS function and response time, and hardware was chosen which supports runtime configurable dynamic range switching. Attention to such details early on allowed us to consolidate hardware in three main categories, served by three different MicroTCA cards.

Full Current Measurement Our beam current monitor (BCM) uses AC-coupled transformers (ACCT) and external trans-impedance amplifier to deliver fast response (>300 kHz analog bandwidth), over 1 mA range, and a unique differential current monitoring scheme for MPS. For this task we selected the [6] Struck SIS8300-L2 10-channel digitizer and FPGA board combined with [7] SIS8900 RTM analog conditioning board.

Low Current Measurement Beam loss monitors such as halo monitor rings, ion chambers, and neutron detectors will generate currents in a lower range, usually less than 100 uA. MPS algorithms involve a configurable integration window combined with configurable threshold limit. Various intermittent-use devices will utilize this same hardware, even though MPS function is not required, including faraday cups and scanning wire profile monitors. We worked with CAENels to provide a customized version of their AMC-PICO-8 MicroTCA board [8], an 8-channel fast sampling picoammeter. Our custom version includes two runtime-selectable dynamic ranges (16 uA and 130 uA) and faster response (DC to 35 kHz) compared to COTS version. CAENels also provided support for integration of custom firmware developed by FRIB for MPS functionality and GTS integration.

Fast Voltage Measurement We have planned many (149) beam position monitors (BPM), each with 4 buttons to digitize at high speed. We will process the 2nd harmonic (161 MHz) of the 80.5 MHz bunching frequency. A system designed specifically for BPMs is required. After investigating several BPM DAO systems, we chose to leverage the same MicroTCA digital board which was used for our EVR card. This is a general purpose digital FPGA board, developed by FRIB for use in multiple applications including machine protection system master and slave nodes, and low-level RF controls hardware. This FRIB digital board may be used either inside or outside a MicroTCA chassis. It made sense to leverage the hardware and firmware expertise already developed in-house to achieve a low cost per-channel, and get a jump start on development. A new RTM board was designed for the BPM application, providing analog signal conditioning and digitization, and designed to interface with the FRIB digital board. The fully in-house development gives us complete control over hardware and firmware design for this critical system.

FIRMWARE SIMPLIFICATION

The three FPGA boards thankfully all utilize common FPGA design tools, as all FPGAs are Xilinx. HDL code is developed modularly when possible to make possible sharing of modules between designs.

To simplify and accelerate development of signal processing algorithms for FPGAs, we have been utilizing the Xilinx Vivado High-Level Synthesis (HLS) tool [9]. It is one of several tools which allows the developer to code C or C++ functions which are synthesized to portable HDL, such as Verilog or VHDL, which can be imported to a larger FPGA project.

A detailed discussion of HLS is beyond the scope of this document, however the attraction of such a tool should be clear: C or C++ offers familiarity and ease of programming in a popular high-level language. Development of signal processing algorithms can be coded effectively in C, and HLS handles the conversion to efficient HDL code, automatically incorporating math IP cores, FPGA resource sharing, pipelining, and timing constraints. As should be expected, there is a learning curve to get started, and this tool does not replace the need for HDL expertise, but such tools can be very powerful to accelerate development of FPGA-based solutions which would otherwise be quite complex in HDL alone. Vivado HLS seems particularly well suited for math-intensive signal processing tasks, accelerating development time and resulting in efficient FPGA resource usage.

SOFTWARE AND DATA REPORTING

As mentioned previously, multiple diagnostic devices which share the same firmware benefit from shared software at the driver level. In an effort to standardize software development further, a common beam data reporting scheme was created, which will apply to all MicroTCA based diagnostics.

A common beam data reporting scheme capitalizes on the fact that no matter what beam mode we are in (CW, pulsed, ramp-up), there is always the 10 msec beam cycle period. This provides a natural time window over which to integrate or average the measurement, and to report simple statistics. Most of our diagnostic devices measure current, so the FPGA firmware will calculate the total integrated current over the 10 msec beam cycle, track min and max values during that period, and report how much time the beam was expected to be on. The software IOC driver will acquire these measurement records at 100 Hz (see Table 3 and Fig. 4), continuously providing 100 Hz sampled data waveforms and also providing further averaging/decimation as desired. For example, a 1 Hz average current value is reported and calculated by averaging 100 of the last 100 Hz average current samples, beginning at the start-of-second GTS event, which is synchronous across all devices.

Table 3: 100 Hz Beam Measurement Rec	ord	
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Beam Measurements @ 100 Hz
Total Charge (integrated current)
Beam ON Time
Average Beam Current (over 10 msec)
Typical Beam Current (during ON time)
Min / Max Current
Timestamp (start-of-cycle)

Calculated offset value may also be included, where the offset is calculated during the 50 µsec diagnostic beam gap, using the previous gap or multiple gap averaging.





The beam position monitor reports different kind of data: X, Y position, magnitude (intensity), and phase. However, BPM will still utilize the 100 Hz period to average and decimate reporting.

All devices will also support triggered acquisitions of N samples, decimated by factor of M, where N and M are configurable and decimation is implemented in IOC software.

All devices also store and continuously update a history of raw data, sampled at 1 MS/sec, for 1 second per channel. This is implemented by local DDR memory on the FPGA board, operated as a ring buffer. This fulfils an MPS requirement that each device reports 1 second of history data preceding an MPS "trip" event when the machine protection system shuts down the beam. An MPS trip will freeze all ring buffers shortly after beam shut down, and the contents of the ring buffers may be examined. Data is timestamped in a synchronous way across the entire machine, made possible by the GTS. Figure 5 illustrates what a portion of the ring buffer might look like after an MPS trip event.



Figure 5: Differential BCM data leading up to MPS trip.

The 1 second MPS ring buffer requires 4 MB per channel, perhaps 8 GB or more for the entire array of diagnostics. It should be noted that to reduce network traffic, the ring buffer memory local to each DAQ card may be masked or ignored, such that only certain devices of interest are read back.

This common diagnostics data reporting structure is easily utilized by high-level software / application developers, and enables straightforward plotting data from multiple different devices on a common time scale.

CONCLUSION

An effort to reduce the number of independent hardware/firmware/software development efforts where possible has enabled a small diagnostics electronics team at FRIB to make fast progress.

A high degree of commonality was achieved for diagnostic DAQ hardware. Three MicroTCA DAQ cards cover about 75% of devices. This led to shared firmware and software development at low-level. Common beam data reporting standards will simplify high-level software development.

Additional factors for efficient development included leveraging existing in-house hardware development efforts (FRIB digital board), good support by industry partners for custom firmware development, and HLS tools to provide accelerated HDL algorithm development using C language.

Proper functioning beam diagnostics are a critical component of the machine tuning and commissioning. We are on our way to delivering high quality beam diagnostics for upcoming front-end commissioning.

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