A FPGA BASED COMMON PLATFORM FOR LCLS2 BEAM DIAGNOSTICS AND CONTROLS*

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Abstract

The LCLS2 is a CW superconducting linac driven X-ray free electron laser under construction at SLAC. The high beam rate of up to 1MHz, and ability to deliver electrons to multiple undulators and beam dumps, results in a beam diagnostics and control system that requires real time data processing in programmable logic. The Advanced Instrumentation for Research Division in the SLAC Technical Innovation Directorate has developed a common hardware and firmware platform for beam instrumentation based on the ATCA shelf format. The FPGAs are located on ATCA carrier cards, front ends and ADC /DAC are on AMC cards that are connected to the carriers by high speed serial JESD links. External communication is through the ATCA backplane, with interlocks and low frequency components on the ATCA rear transition module (RTM). This platform is used for a variety of high speed diagnostics including stripline and cavity beam positon monitors (BPMs).

KEY FEATURES

A new instrumentation / control platform has been developed for LCLS2 in order to provide the following features that were not all available with existing platforms:

- Ethernet communication within a c to simplify hotswapping and control of distributed systems.
- Timing data stream distributed to all application cards to allow beam parameter dependent processing.
- Analog front ends integrated with ADCs / DACs, but separate from digital systems to allow digital and analog engineers to work independently and to provide independent upgrade paths
- Large application card area with vertical space for RF shielding to simplify the design of high performance RF systems
- High system density with efficient use of rack space for analog connections.
- Widely-used telecom hardware.

HARDWARE OVERVIEW

The "Common Platform" is based on the Advanced Telecommunications Computing Architecture [1] (ATCA) that is widely used in industry. The SLAC common platform is based on the following components (figure 1, 2):

- ATCA Shelf: This is the "crate" that holds the electronics cards, power supplies, etc.
- Backplane: Provides high speed data connections from all cards to slots 1 and 2.
- Management: Provides IPMI for shelf components (commercial)
- Network Switch: This is an ATCA carrier card that is located in slot 1 with access to Ethernet to each carrier card, and which provides a 10Gb, or 40Gb uplink. (typically commercial, custom also available)
- Carrier Card: This card contains a FPGA and has serial connections to the backplane Ethernet, and to the RTM and dual AMC cards. The carrier card also contains DC-DC power supplies from the -48V to a variety of voltages used by the AMC cards.
- AMC card: These contain the analog front ends, ADCs and DACs, and timing chips
- RTM card: These are connected directly to the FPGA on the carrier card and are used for miscellaneous I/O and network connections.

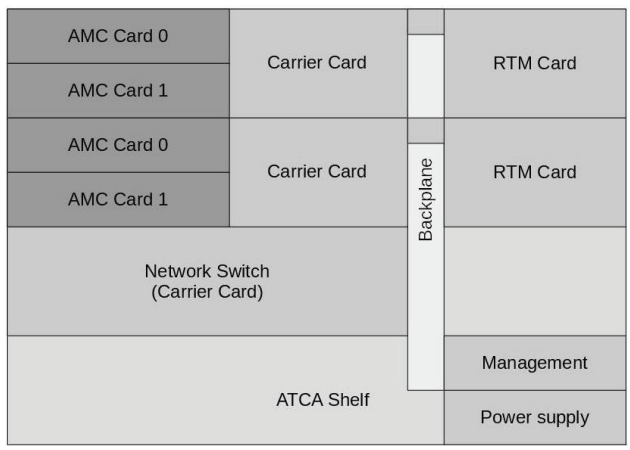

Figure 1: Common platform components.

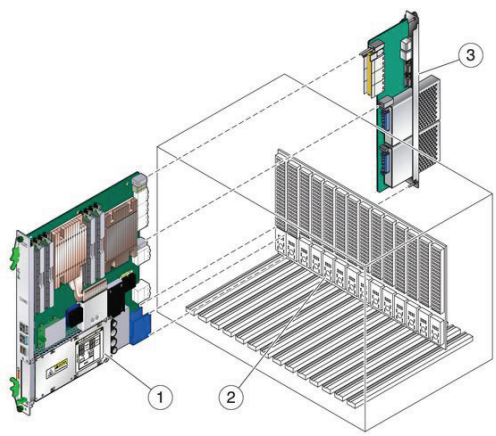

Figure 2: ATCA shelf and cards.

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HARDWARE DESIGN

The high average throughput required for LCLS2 instrumentation necessitates the use of programmable logic for processing data. The digital and analog portions of the design are separated, with. the FPGA, memory and network interfaces on the carrier card.

Each carrier card supports two, double-width, full-height AMC daughter cards. The AMC slots are backwards compatible to support standard ATCA cards, but include extra DC power supplies on otherwise unused pins. (These supplies are controlled through IPMI and only activated with compatible AMC cards).

The use of full height AMC cards provides extra vertical room for RF shielding for noise sensitive systems and extra front panel connector space.

The choice of ADCs / DACS is generally tied to the required analog bandwidth and dynamic range requirements, so they are included on the AMC cards. Most AMC card ADC / DACs use JESD204b [2] serial interfaces, however parallel digital is also supported.

The system is designed to minimize network cables. The ATCA backplane carries primary data communication, management, machine protection data, and a timing data stream to each carrier. In a typical configuration only analog signal cables are required to the application cards.

The RTMs provide extra connector space for special purpose networks, and general purpose low speed analog and digital. If only a single carrier card is required in one location, the networks can be directed to the associated RTM card, eliminating the need for a network switch in the shelf. This allows operation in a NAD-like configuration.

The ATCA standard provides a number of useful functions:

- Hot swap for carrier cards and RTMs. This allows the use of multiple functions in a shelf without interfering with maintenance.
- System management and monitoring.
- High speed (10Gb) networking with future upgrade paths.
- Temperature rating 50°C
- A variety of shelf sizes from 1 slot to 14 slots, with vertical and horizontal orientations.
- Ethernet backplane communication which simplifies dividing systems between multiple shelves.

BACKPLANE / NETWORKS

The Common Platform uses a standard dual-star configuration of an ATCA backplane. This provides the following networks (figure 3)

- 10Gb Ethernet (4 lanes) from slot 1 in a "star" to all other cards. This is the ATCA "fabric" network. It is used for general high speed data transmission to the Ethernet switch located in slot 1.
- One lane from slot 2 in a "star" to all other cards. This is used for the serial timing data stream. This is part of the 2nd ATCA "fabric" network.
- One lane from slot 2 in a "start" to all other cards. This is used for Machine Protection System data. This if part of the 2nd ATCA fabric network.
- IPMI to all slots for configuration / monitoring.

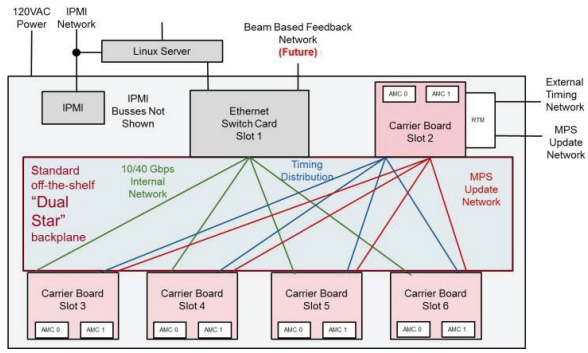

Figure 3: Common platform networks.

CARRIER CARD DESIGN

The SLAC-designed carrier card is based on a Xilinx *Kintex Ultrascale* XCKU040 or XCKU060 FPGA, the latest generation of chips available when the design was frozen. The FPGA is interfaced to 8GB of DDR3 memory, and to the networks described in the previous section (figure 4).

Each AMC daughter card uses dual 172-pin connectors (ATCA B+ AMC) rated to 12.5Gbit. The XCK040 FPGA provides 7 bi-directional serial lanes (typically configured as JESD204b) to the carrier card, the XCK060 (same package) provides 10 lanes. This provides a total data rate from ADCs of 87.5Gb/s or 125Gb/s. With typical 8b/10b encoding that supports 4.3Gs/s of 16 bit ADCs with the smaller FPGA and 6.25Gs/s with the larger. Simultaneous use of full data rate on ADCs and DACs is supported.

The carrier card includes DC-DC converters from the shelf -48V to its internal supplies and supplies to the AMC cards. For most designs this eliminates the need for DC-DC converters on the noise sensitive AMC cards.

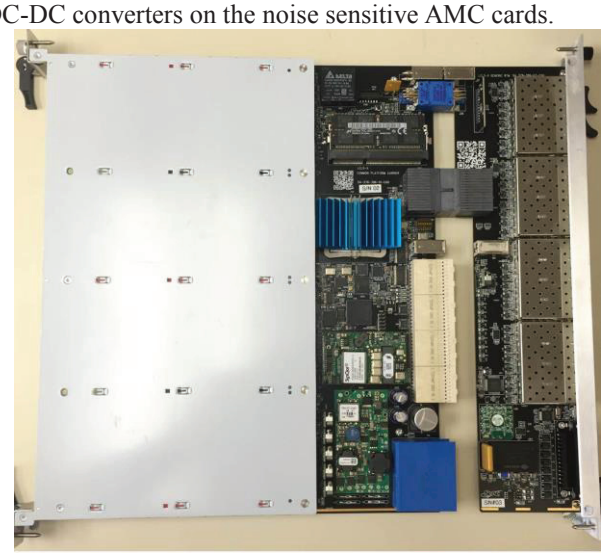

Figure 4: Carrier Card, FPGA is under blue heat sink. Network RTM card is attached on the right.

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AMC CARDS

The AMC cards are 148.5mm X 180.6mm, with approximately 20 mm of clearance above the boards for components and shielding. AMC cards include analog electronics and ADC / DACs. A number of AMC cards are under development for LCLS and LCLS2.

General Purpose ADC / DAC Card

This card is intended for applications requiring high performance ADCs / DACs. This includes:

- IF digitizers for cavity BPMs,
- Toroid readouts
- Bunch length monitor readout based on Coherent Synchrotron Radiation (CSR)
- Radiation monitors (fibers, ion chambers etc.)

The card contains four channels of 16 bit, 370Ms/s ADCs. One of the digitizers is used to measure an internally generated trigger to correct for the clock vs trigger timing in the algorithm.

The card also contains 2 channels of 16 bit, 370Ms/s DAC for signal generation, and general purpose digital and fiber outputs.

The general purpose cards are complete, and being used for development of LCLS2 beam instrumentation.

Stripline BPM

This card contains bandpass filters (typically 60MHz bandwidth around 300MHz), Variable gain amplifier chains, and calibration circuits,

It uses the same 16 bit 370Ms/s digitizers as the general purpose card, but operating in the second Nyquist band. Prototype BPM cards are currently being tested.

LCLS1 LLRF System

The LCLS 1 room temperature LLRF system is being upgraded to modern hardware. A pair of AMC cards and an RTM on one carrier card provides RF control, read back and fast interlocks for a standard LCLS1 RF station. [3].

The system provides ten channels of LLRF input with downmixers, and LO generation. The digitizer clocks and LO used FPGA based PLLs to allow locking to the accelerator reference RF and timing system. The firmware allows locked or unlocked operation [4].

Changing a few components (filters and RF splitters) allows the card to operate from 400MHz to 3GHz.

Prototypes have been tested with a measured phase noise at 2856MHz of < 0.005ºRMS in a 1MHz bandwidth.

In addition to use on the LCLS LINAC, this system is being used for the SPEAR Booster upgrade, and is planned for use on the SPEAR ring RF upgrade in the future. A 1300MHz version for superconducting RF systems has also been tested with good performance.

TIMING SYSTEM

A new timing system has been developed for the LCLS2. It consists of a 3.7Gb/s data stream which uses 8b/10b encoding to provide 16 bit words at the 185.7 MHz reference clock frequency, corresponding to the 1300MHz accelerator frequency / 7, the same as the injector RF gun frequency.

The timing data is transmitted in 3200 bit frames, at a frame rate of 928kHz, corresponding to the maximum beam rate in the LCLS2. The bits in each frame contain information about that beam pulse, including pulse ID, destination, requested charge, and markers for 60Hz power line synchronization. The frame also contains a bit "pattern" that specifies when each triggered device should operate.

The timing data stream is distributed by an external fiber network to a carrier card in slot 2 of each ATCA shelf. From that carrier card, the data stream is transmitted on the ATCA fabric (1 lane) to all carrier cards. The data is transmitted approximately 100us in advance of the beam, allowing time for transmission delays in the 4km long accelerator system and for processing / triggering in advance of beam pulses.

The FPGA on each carrier card contains firmware to decode the data stream. This serves multiple functions:

- Tag data with a pulse ID for non-realtime applications.
- Modify processing algorithms based on beam destination or parameters.
- Provide external hardware triggers
- Provide internal triggers in firmware or hardware for signal processing.
- Provide a distributed check that the beam is being directed to the correct destination.

The Common Platform hardware and firmware can also decode the data stream from MRF timing systems [5], allowing its use in LCLS1 applications. The frequencies of LCLS1 and LCLS2 are harmonically related and in the future the LCLS2 timing system will be able to perform all functions required for both systems.

FIRMWARE

The Common Platform firmware is written in a modular fashion to allow signal processing / application development to be done independently of platform / communication firmware (figure 5). Most application development is done in Mathworks Simulink with Xilinx System Generator [6].

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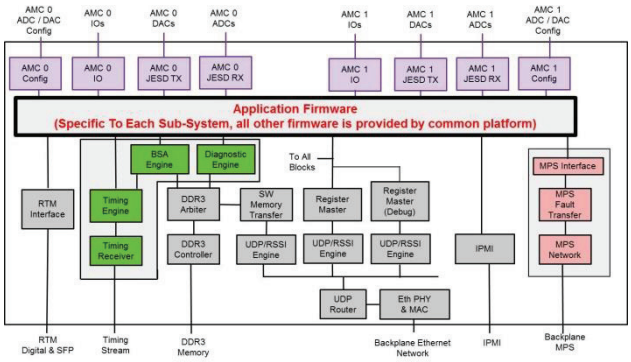

Figure 5: Firmware block diagram.

MACHINE PROTECTION

The LCLS2 fast machine protection system makes use of the Common Platform hardware and firmware. Each instrumentation card (BPM, etc.) compresses its data, associates it with a pulse ID from the timing system, then transmits the data on the backplane to a card in slot 2, using the MPS network, which is not shared with any other traffic. From there the data is sent on a private network to the mitigation nodes which run the MPS algorithm and either reduce beam rate or shut off the beam.

Since each card has the timing data, and that data includes the beam destination, all BPMs can locally check for beam present in the wrong line, or lack of beam when it should be present. This provides an independent check that the various system kickers are responding correctly to the timing patter request.

The slot 2 MPS card is a standard SLAC carrier card running a simplified set of firmware which transmits the MPS data.

OTHER APPLICATIONS

The Common Platform system is generally useful for applications requiring high throughput real time data processing in a compact high reliability form factor.

An example application is the RF system for a Transition Edge Sensor using a microwave multiplexer. This sensor is intended for a variety of applications including high energy resolution X-ray imaging and cosmic microwave background measurements [6].

The sensor array is operated at ~100mK temperatures, which each pixel coupled with a SQUID to a resonant circuit in the 4-8GHz frequency range. Measurements are made by tracking changes in the resonance frequencies of the sensor. The electronics must generate a comb of RF tones to drive the sensor, each tone being tuned to track the pixel resonance.

The common platform implementation of this uses a pair of AMC cards on a carrier to provide 4GHz bandwidth of signal generation and measurement in a 4-8GHz frequency range. Each AMC contains 2, dual channel 3Gs/s digitizers with internal DDC, and 2 dual channel 3Gs/s DACs with DDS, along with band selection multiplexers, and local oscillators. The FPGA will generate tones to track up to 4000 resonances.

Electronics / RF design of this system is nearing completion, with first hardware expected in late 2016.

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