THE SLAC LINAC LLRF CONTROLS UPGRADE*

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Abstract

The low level RF control for the SLAC LINAC [1] is being upgraded to provide improved performance and maintainability. RF control is through a high performance FPGA based DDS/DDC system built on the SLAC ATCA common platform. The klystron and modulator interlocks are being upgraded, and the interlocks are being moved into a combination of PLC logic and a fast trip system. A new solid state sub-booster amplifier will eliminate the need for the 1960s vintage high RF phase shifters and attenuators.

OVERVIEW

The legacy RF system at SLAC has been in operation for over 50 years. Despite working extremely well for many years, many parts of the system are showing signs of wear including effects as esoteric as copper erosion in some water cooled chassis. A rough block diagram of the legacy RF system is shown below in Fig. 1.

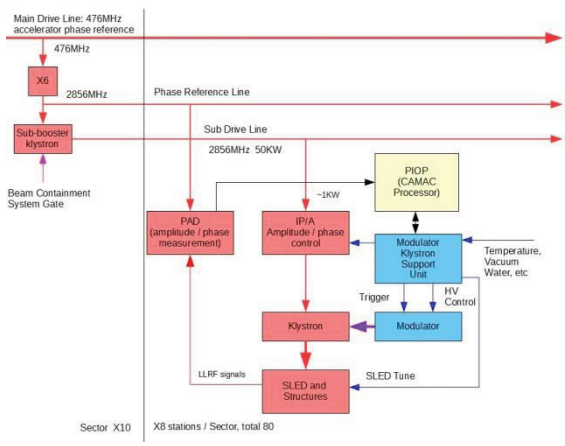

Figure 1: Legacy RF system.

To mitigate these effects and to provide for upgradeability well into the future, the US Department of Energy is investing in upgrading the system using modern FPGA based technology. When upgrading a system such as this, many conflicting requirements must be met at once. During the design process, many platforms were evaluated for applicability and maintainability. We evaluated: VME, PXI, mTCA for physics, ATCA, and conventional chassis. At the same time this evaluation was going on for LLRF upgrades at SLAC, the diagnostics, machine protection and other groups were evaluating their own common platform solution and had decided on ATCA as their platform of choice. Because of that decision and our own evaluations, it was decided that the system will be designed into the ATCA platform. A high level block diagram of the new LLRF system is shown in Fig. 2.

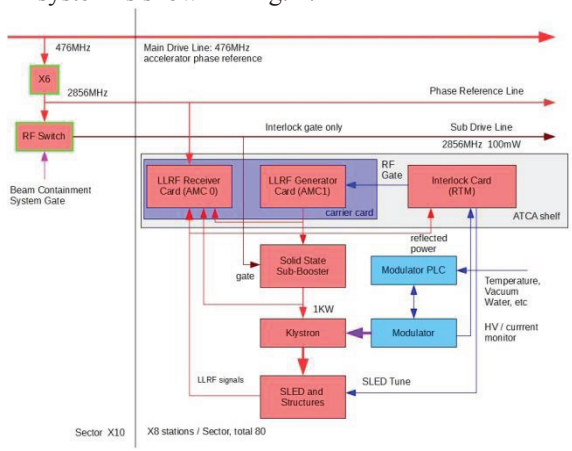

Figure 2: Upgraded RF system.

DETAILS OF NEW SYSTEM

The system is being designed into a new platform based upon the telecommunications system ATCA [2]. The system incorporates two advanced mezzanine cards (AMC cards) which plug into a carrier card that contains the FPGA for all signal processing functions. The overall common platform system allows for enough flexibility that the design can be used for other diagnostic and machine protection functions simply by designing other AMC cards with the specific functionality required for those systems. Further details of the common platform system are covered at another paper in this conference [3].

Specifications and Backwards Compatibility

The LLRF system has to completely replace the old system which was based upon CAMAC controls and other custom chassis within the larger LINAC system. In addition, the system will not be able to be upgraded as a whole at one time; the design incorporates a method for upgrading as little as one station at a time. To that end, there are several requirements on the new system for it to fit into the existing infrastructure of beam containment (BCS), timing systems and other legacy systems:

- The new system must maintain compatibility with the existing BCS system without compromising the beam containment functions as currently implemented.
- The new system must replace the legacy Modulator Klystron Support Unit (MKSU) that serves to protect the high power pulsed klystrons and modulators.
- The new system must use solid state sub-boosters for each Klystron, rather than the legacy sector (8 klystron) sub-booster klystron.

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In addition, this new system has to meet or exceed the old electrical specifications of the legacy system. The important specifications are shown in table 1.

Table 1: System Specifications

SPEC	VALUE
Noise (phase)	< 0.01 degrees 1 MHz BW
Noise (amplitude)	< 0.01% 1 MHz BW
Drift (phase)	0.1 degrees
Drift (amplitude)	0.1% (1min) (2 degrees C)
RF Channel Bandwidth	>10 MHz
RF Channel Resolution	16 bit resolution
Non-linearity	0.1 degrees for 6 dB change
Modulator Voltage Readback	14 bits resolution

One final requirement was that the system be capable of handling all current and future RF frequencies used at SLAC (LCLS I - 2856 MHz, LCLS II – 1300 MHz, SSRL Booster – 358.54 MHz, SSRL Ring – 476 MHz).

Detailed Hardware Description

In order to provide enough channels for all potential uses, we determined that 10 channels of RF down-conversion, 1 Channel of RF up-conversion and 2 Channels of Baseband signal detection were necessary. It was further determined that the interlock functions previously handled by the MKSU would be split between a new ATCA rear transition module (RTM) and the klystron modulator control PLC. A more detailed block diagram of the final implementation is shown in Fig. 3.

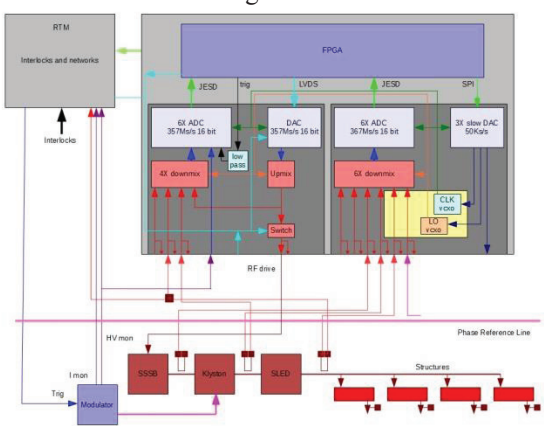

Figure 3: Detailed block diagram.

To enable handling of the multiple clocks and LO's necessary to down-convert all SLAC frequencies it was decided that a daughter card piggy-backed on one of the AMC cards would be used to provide clock and LO signals to both AMC cards. A new pulsed solid-state sub-booster amplifier will be designed to drive each of the 8 klystrons per sector.

AMC Cards The two AMC cards will use the same basic architecture throughout. Each card will contain 3 ADC chips running at approximately 350 Msamp/sec (depending on input frequency). Each chip contains 2 ADCs for a total of 6 ADC channels per board. Because there simply was not enough pins to run parallel bit ADCs we chose to use the relatively new standard of JESD204B serial lanes.

We further broke the design down into what we called a precision card and an up-converter card. The Precision card will be used for comparing critical feedback signals to a reference signal from a phase reference line as shown in Fig 2. This is similar to what the LLRF team designing the LCLS-II system is doing, however we are doing it for differing reasons. Our main reason for splitting the cards in this manner is to get the maximum dynamic range achievable without interference from the signal generation card. Any other precision signals should be input to this card as well. The up-converter card will be used to create the corrected (or feedback) signal that will be fed to the structures (or cavity) depending on application.

The precision card contains six identical RF down-converters with a block diagram as shown in Fig. 4.

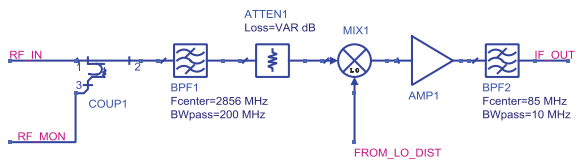

Figure 4: RF Down-converter block diagram.

The up-converter card contains 4 down-converters identical to the ones used on the precision card as well as two buffered baseband signals. One of the baseband signals will be used to monitor the klystron modulator voltage and the other is used internally for timing synchronization of the RF pulse amplitude. The up-converter card also contains a 16 Bit parallel DAC. We had to use a parallel DAC instead of a JESD204B DAC because during initial testing we found excessive latency with the original DAC we had planned on using. The DAC outputs an IF at approximately 85 MHz (depending on application) and uses the same LO as the down-converters to up-convert to 2856 MHz.

Solid State Sub-Booster (SSSB) The purpose of the SSSB is to provide enough input power to drive the linac klystrons to their rated output power with minimal phase noise degradation and reliable long term performance. The SSSB is required to produce up to 1kW pulses 5 us in duration at up to a 240 Hz rate (standard operation is 120 Hz). We are planning to use a hybrid approach of buying GaN-HEMT amplifier modules (bricks) from an outside vendor and installing them into a custom chassis that will be contained in the same rack as the rest of the LLRF system. Interlock RTM The interlock rear transition module's, (RTM) main function is to protect the klystron from various conditions that could result in destruction of the klystron. Previously this was all handled by the MKSU with only a trigger going from the MKSU to the klystron modulator. The new interlock RTM will handle the fast interlocks while the slow interlocks (water, vacuum, Magnet,

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temperature etc.) will be handled in the modulator itself. Fig. 5 shows a block diagram of the interlock scheme.

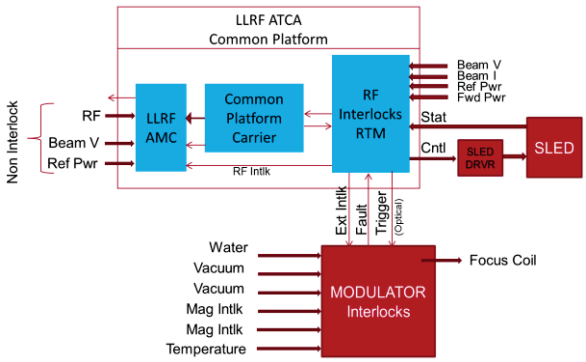

Figure 5: Interlock scheme.

Detailed Firmware Description

The firmware for the LLRF scheme for the SLAC LINAC is a very complex design with many facets (Timing, amplitude and phase adjustments). Over the many years of SLAC operation, many feedbacks have been added on top of the original system to allow for much more stable operation than the original SLAC linac and as a result, the new system must fit seamlessly into those feedbacks with no adverse effects.

All of the main controllability of the system relies on individual klystron phase and amplitude control. To achieve this, a fiducial riding on top of the 476 MHz was used to time the pulse with the arrival of the beam. In that way there was a guarantee that the trigger would be timed in phase with the RF signal being amplified and distributed to the structures of the main linac. With the addition of LCLS-I to SLAC, a new even system was added [4] which essentially split the timing into two differing systems; One being the fiducial system and one being the event system. The event system is used to time a myriad of other systems around the machine (BPM's cameras etc) One goal of this new system is to combine the timing into one system only with a fiber going to each station with the timing information and as a result complicates the firmware implementation.

To achieve pulse to pulse timing stability of less than 100ps on the envelope of the RF, we need a way to detect the trigger at much less than the roughly 2.7ns time allowed by our system clock. To achieve sub-clock sample timing, a novel interpolation scheme was created by running the trigger through a low pass filter, sending to an ADC and then using DSP interpolation to detect the zero crossing with sub time sample resolution. This new timing information is then used to create an interpolated baseband signal which is multiplied (digitally) onto a digitally controlled oscillator which is phase locked to the incoming phase reference IF. A block diagram of the overall firmware scheme is shown in Fig. 6.

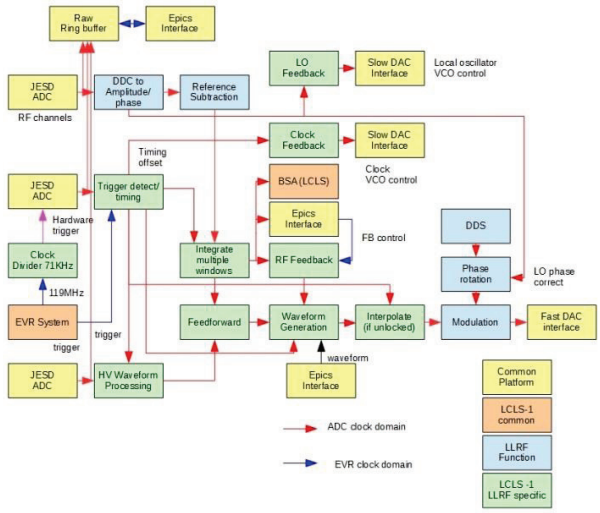

Figure 6: Detailed firmware block diagram.

PROTOTYPE RESULTS

Prototype cards for the LCLS-I LLRF system have been built and initial firmware has been developed to allow for data taking and offline data processing. We present some of the results here.

Phase Accuracy To measure phase accuracy, a common signal is sent into two channels of down-conversion, sampled at an IF/Sample ratio of 5/21 (for near IQ sampling [5]. The near IQ down conversion is filtered by a simple 21 average filter and then digitally down converted to baseband. The LO is locked to the IF of the incoming 2856 MHz signal and the clock is locked using one ADC channel which is sampling an external 119/7 MHz signal (derived from the 2856 Mhz. The locking and measurement scheme is shown below in Fig. 7.

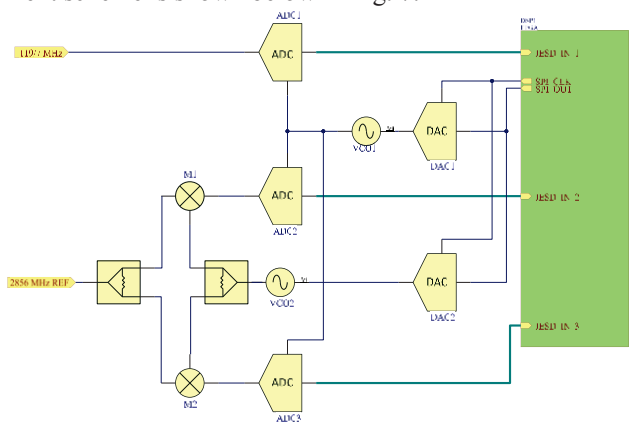

Figure 7: Phase measurement and locking scheme.

To calculate the base phase error, the two IQ signals from ADC2 and ADC3 are converted to phase and amplitude using a cordic algorithm in matlab. The phase signals are then further filtered with a 1MHz lowpass butterworth filter to approximate the final processing band bandwidth. An FFT of the single side band (SSB) results are shown below in Fig. 8. The LO and Clock used in our system while fairly low noise should not be considered phase noise. By using the phase subtraction technique we get

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several orders of magnitude improvement by the subtraction of common noise. In fact, the LO and Clock can be run open loop with reduced performance. Further processing this data shows an RMS phase error of 0.0052 degrees integrated from 100 Hz to 1 MHz this was measured at an intermediate fan speed.

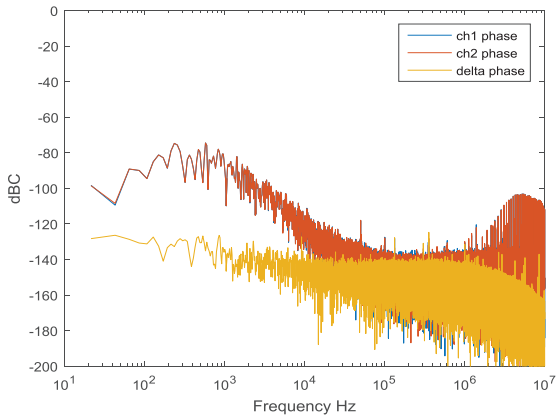

Figure 8: SSB difference phase noise plot.

Amplitude Accuracy Using the amplitude data from the algorithm mentioned in the phase accuracy section, we calculate at ch1 and ch2 amplitude errors at 0.0093 and .0096% respectively.

Output Phase Noise The output phase noise of the system must also meet very stringent requirements. To verify the performance we generated an output signal at 2856 MHz using prototype firmware. The SSB output phase noise as measured by an Agilent E5052B phase noise analyser is shown below in Fig. 9.

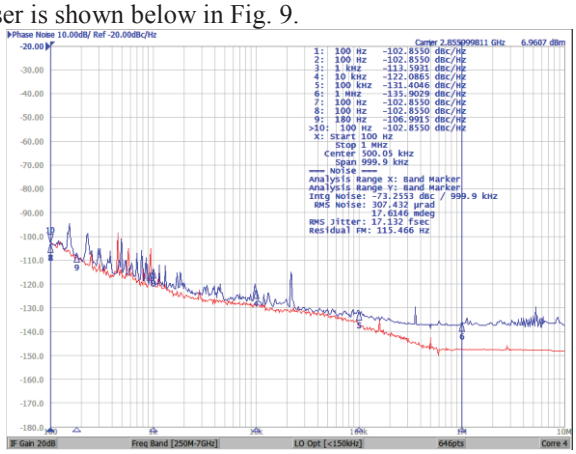

Figure 9: 2856 MHz output phase noise.

The red line in Fig. 9 is the input reference noise. The blue line is the output phase noise which tracks the input phase noise quite well up to around 100 kHz at which point it becomes dominated by the noise floor of the output circuitry. This needs further investigation. The integrated rms noise from 100 Hz to 1 MHz is 0.0176 degrees.

Other Performance Tests One particular test meriting investigation is potential phase degradation under full ATCA fan speed. We ran the system at full fan speed and did, in fact, see a degradation of the phase noise. However, as can be seen in Fig. 10, the full integrated phase noise is still below the 0.01 degree phase specification. To further mitigate this problem, we are planning on testing some dampening material on the oscillator daughter card as we expect that vibration on that card may be contributing to this added phase noise.

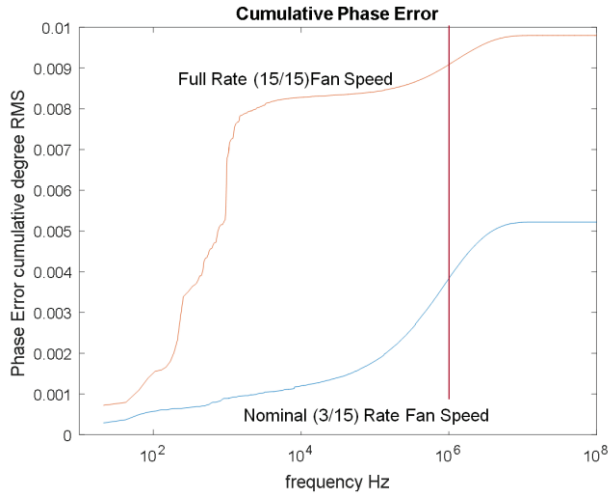

Figure 10: Phase error at full fan speed.

CONCLUSIONS

We have designed and tested prototype hardware for the LINAC upgrade project at SLAC. Testing to date shows that the system as currently built nearly meets all specifications. The layout designs of the two AMC cards are in the process of being modified as of the writing of this paper. The new boards are expected to be tested on beam later this calendar year to show full proof of concept prior to moving into production mode and installation into all 80 RF stations contained within the LCLS-I LINAC.

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