BATCH APPLICATIONS OF DIGITAL BPM PROCESSORS FROM THE SINAP *

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Abstract

During the past several years a digital BPM (DBPM) processor has been developed at the SINAP. After continuous development and optimization, the processor has been finalized and has come to batch application on the signal processing of cavity BPMs and stripline BPMs at the Dalian Coherent Light Source (DCLS) and the Shanghai Soft X-ray FEL (SXFEL). Tests have been done to evaluate the performances, such as the noise level, the SNR and the cross talk. The system resolution of the cavity and stripline BPMs can achieve 1um and 10um respectively. The test results on the Shanghai Deep-Ultra-Violet (SDUV) and the DCLS will be introduced.

INTRODUCTION

A prototype of the DBPM has been developed successfully at the SINAP during the past few years [1~5]. Some tests and applications have been carried out at the Shanghai Synchrotron Radiation Facility (SSRF)[6]. Since 2015, two FEL facilities, DCLS and SXFEL, have been under constructions. Dozens of stripline BPMs and cavity BPMs are planted along the LINAC accelerators and the undulators. To handle the BPM data acquisitions and the position calculations, a new in-house BPM processor has been designed.

The main system structure of the previous DBPM has been kept for the new design, and some optimizations and modifications are implemented aiming at the application on FEL. Figure 1 is an overview of the system structure. It consists of 4 input RF signal conditioning blocks, 4 analogue to digital converters (ADC), a digital signal processing module, and a CPU running control system.

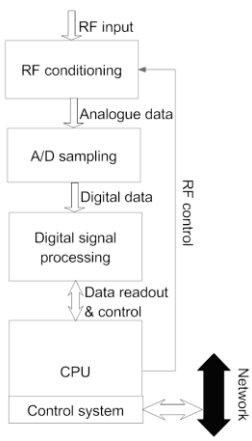

Figure 1: DBPM processor architecture.

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HARDWARE DESIGN

The processor includs four input channels, and it mainly consists of three boards: a carrier board implementing the RF conditioning and digitizer with ADCs, a mother board holds FPGA and other peripheral components and interfaces, and an ARM board conducting system control (as shown in Figure 2).

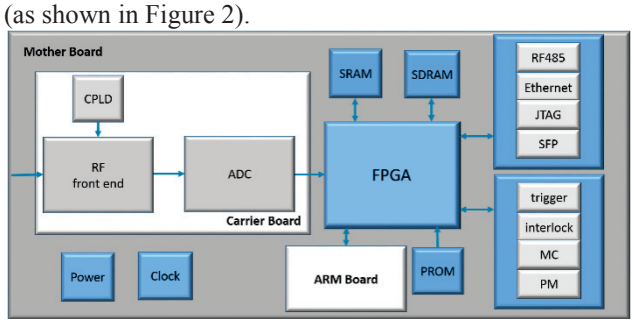

Figure 2: Hardware diagram.

RF Carrier Board

There are four input channels on RF carrier board. Each channel has two functions: the RF conditioning and the ADC digitizer. Figure 3 is the signal conditioning flow of one channel. The brief descriptions are:

- Two surface acoustic wave (SAW, TFS500A) bandpass filters, whose centre frequencies are 500MHz and their 3dB bandwidths are 12MHz.
- Three low pass filters (LFCN-575) located at different processing sections.
- Three fixed amplifiers and one 31dB digital step attenuator with 31dB dynamic range, which is controlled by a CPLD on the board.

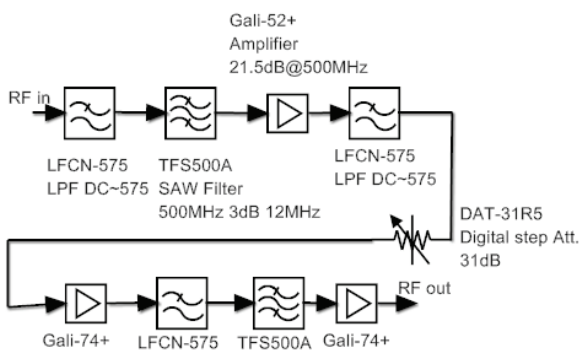

Figure 3: RF conditioning flow.

After conditioning, the RF signal is digitized by a 16bits ADC at the rate is 117.2799MHz. Clock source can be selected to be internal or external.

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Mother Board

The main components on the mother board are: a Xilinx FPGA chip XCV5SX50T, a couple of DDR2 SDRAMs, a power supply, an RF board connector, an ARM connector, an Ethernet port, a UART port, and an external I/O. The FPGA and the ARM communicate through the 1x PCIE bus, The RF board is controlled by the FPGA through the SPI bus, as shown in Figure 4.

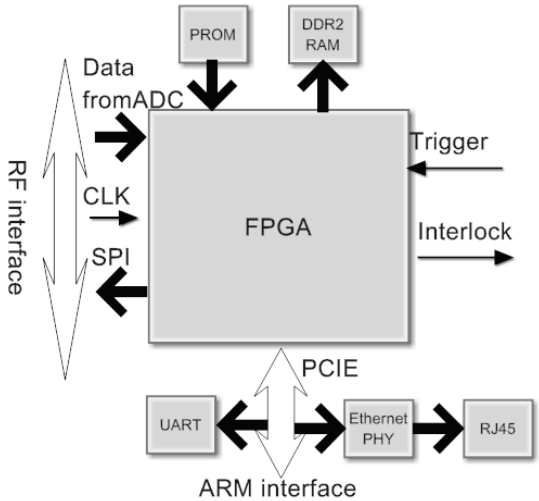

Figure 4: Mother board hardware block diagram.

ARM Board

An IMX6Q is chosen to act as a system controller. The IMX6Q is set to boot from an SD card, therefor it is convenient for batch production.

Figure 5 is the hardware pictures.

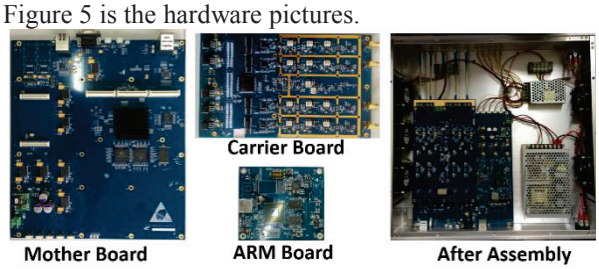

Figure 5: Hardware pictures.

FIRMWARE AND SOFTWARE DESIGN

System interfaces and signal processing functions are implemented on the FPGA. As illustrated in Figure 6, the firmware design on the FPGA includes an SPI interface with an RF board, a PCIE interface with an ARM board, 4 ADC data inputs, clocks, RAM interfaces, and an innovative self-trigger module. The self-trigger module detects the pulse arrive time and generates trigger signals when the beam passes the BPM pickups. After the trigger, a 4×2048 points FIFO in the FPGA will capture four channels of 1024 points data before and after the trigger separately. Once the FIFO is full, the FPGA will send out a sign to the ARM and restart a new cycle after the data is read out. This design enables the system work without external trigger input and improves the adaptability. Figure 7 is the function illustration of this module.

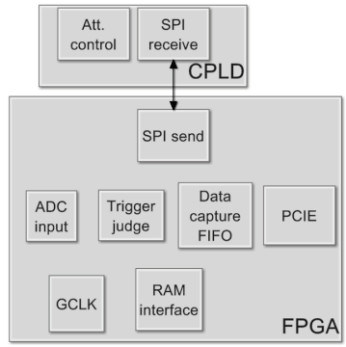

Figure 6: Firmware structure.

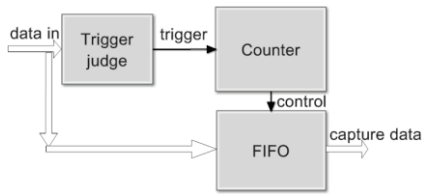

Figure 7: Self-trigger module.

The IMX6Q on ARM board runs ARM Linux OS and EPICS control system. Raw data read from FPGA is processed on IMX6Q because of low beam rate at 50Hz. Figure 8 is the EDM configure panel. Both Hilbert and FFT algorithms are implemented for user selection to calculate the amplitude and the phase on each channel. And different position calculations are supplied according to different BPM types. At the same time, the processor can be set to work with external or internal trigger.

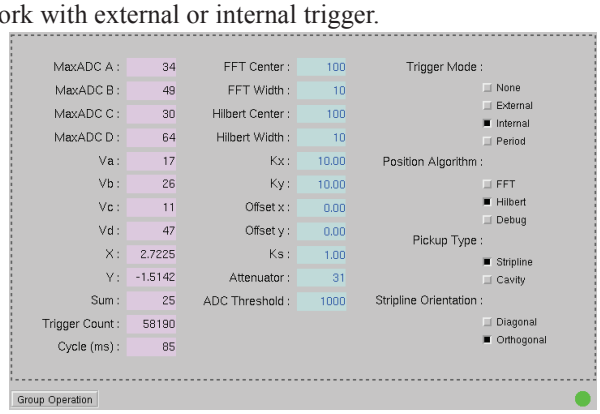

Figure 8: Configure panel.

AUTOMATIC TEST PLATFORM AND PERFORMANCE EVALUATION

Dozens of processors are used at the DCLS and the SXFEL. Manual lab test of this large amount of instruments is tedious and time consuming. An automatic test platform described in Figure 9 has been designed to improve the test efficiency. A PC running Matlab and EPICS controls the RF output signal source and the DBPM attenuator settings through TCP/IP protocol.

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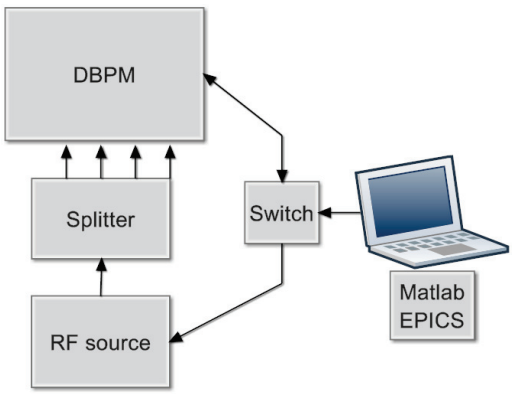

Figure 9: Automatic test platform.

Figure 10 shows the test results of one processor. Figures (a) and (b) show that the noise level and the crosstalk keep almost the same low level when the attenuator is set to be 16~31dB. Figure (c) shows the good linearity between the setting and the output of the gain. Figure (d) indicates that the SNR can be better than 76dB, which means that the effective bits is greater than 12bits.

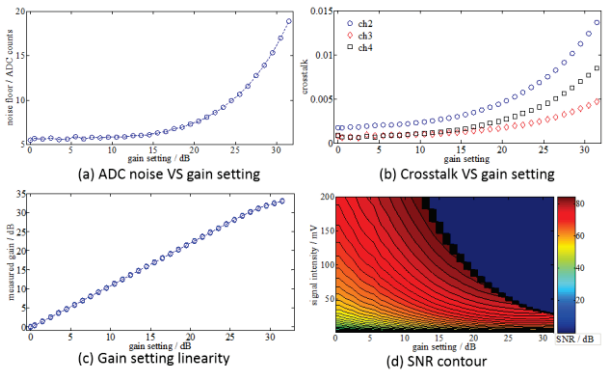

Figure 10: Performance test results.

TESTS AT THE SDUV

The SDUV is an FEL test facility in SINAP. Three adjacent cavity BPMs are installed on the LINAC accelerator to evaluate the performance of the cavity BPM system.

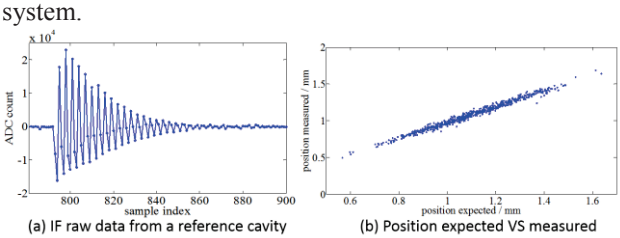

Figure 11: Test results on SDUV.

Test results show that DBPM can capture the cavity BPM intermediate frequency (IF) signal correctly, and the resolution can be better than 1 μm, which reaches the performance requirement of the cavity BPM system.

APPLICATION AT THE DCLS

There are 8 stripline BPMs and 10 cavity BPMs at the DCLS. All DBPMs are installed in this July. Figures 12 and 13 are the pictures of the batch production and application of the DBPM at the DCLS. Because the accelerator is still under commissioning, precise BPM system performance evaluations will be carried out in the future.

Figure 12: Batch production and application on DCLS.

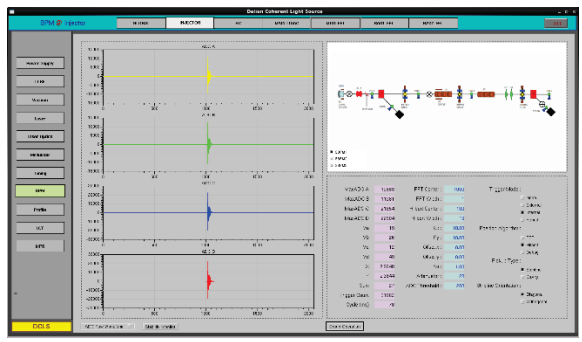

Figure 13: DCLS BPM panel.

CONCLUSIONS

A new DBPM processor has been designed for both stripline and cavity BPM. The effective bits can be greater than 12 when the input signal level and attenuation value are fitted. SDUV tests show that the DBPM works correctly. DBPMs have been applied on DCLS, system performance evaluations will be carried out in the future.

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