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TURN-BY-TURN TIMING SYSTEMS FOR SuperKEKB DAMPING RINGPOSITION MONITORS

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Abstract

Turn-by-turn timing systems for SuperKEKB beam position monitors using Xilinx Zynq FPGA have been developed. The RF frequency divider with external synchronization circuit creates a fiducial signal synchronized to the accurate injection timing from the injector event system. As the Log-Ratio turn-by-turn monitors (Digitex 18k11) need clock timing deviation to the beam signal within 8 ns, the cable length from the BPM heads to the detectors have been adjusted with the maximum deviation less than 1 ns using TDR. The time delay to adjust each cable lengths and the BPM placements have been created by using 32-ch RF timing delay with the step of 2 ns. The start trigger to the 18k11 has been made by using the digital delay (SRS DG645) from the injection trigger. The measured performance of the frequency divider, the 32-ch RF timing delay and start trigger system will be shown.

INTRODUCTION

The KEKB collider has been upgraded to the SuperKEKB collider with a final target of 40 times higher luminosity than that of KEKB. It consists of a 7 GeV high energy ring (HER, electrons) and a 4 GeV low energy ring (LER, positrons). About 2500 bunches per ring will be stored at total beam currents of 2.6 A (HER) and 3.6 A (LER) in the final design goal.

Due to strong focus at the interaction point, the dynamic apertures of both rings will be spoiled with the squeezing of the beam. To cure the LER injection efficiency and to reduce the beam noise coming from injected beam, the positron damping ring (DR) has been constructed in the linac with energy of 1.1 GeV after the production target, to damp the emittance of the positron beam. Table 1 shows the main parameters of the SuperKEKB damping ring.

Since the beam circulating time in the normal operation is short, from 40 ms to 200 ms depending on the injection repetition, and since the bucket filling pattern and injected bucket changes due to the bucket selection system to fill the beam as uniform as possible at LER, we have decided to use turn-by-turn beam position detector with Log-Ratio detection scheme using Digitex 18K11 [1]. As it is the time-domain detection system, we need to prepare following timing signals:

- Position data acquisition start trigger with good time relationship from the injected beam.
- Master clock timing for the ADC of 18K11 (Fiducial, 2.21 MHz) synchronized to the measuring bunch.
- Delayed timing to compensate the BPM placements in the ring and cable delays for each BPM.

To generate such timing signals, we have developed following timing generation circuits:

- RF frequency divider with external synchronization circuit using Zynq FPGA.
- Multi-channel (32-channels) digital delay working with the RF timing using Zynq FPGA.
- Start trigger generator with fine digital delay starting from the external signal (injection timing) under the software control (enable /disable start).

The measured performance of the systems such as the jitter of the timing will be shown in this paper.

Table 1: Major Parameters of SuperKEKB Rings

	DR
Energy (GeV)	1.1
Circumference(m)	135.5
Max. Beam current (mA)	70.8
Max. Number of bunches	4
Bunch separation (ns)	>96.3
Natural bunch length (mm)	6.5
RF frequency (MHz)	508.887
Harmonic number (h)	230
T. rad. damping time (ms)	11
x-y coupling (%)	5
Beam emittance at Inj (nm)	1700
Equilibrium emittance (nm)	41.4/2.07
Max. injection rate (Hz)	50
Number of BPMs	83
Number of BPM stations	4

BEAM POSITION MONITORS

Since the storage time of a beam in DR is normally short, less than 200 ms, we have constructed the turn-by-turn based beam position monitor systems with Log-Ratio detector (Digitex 18K11). From the measured narrow pulse response of 18K11 detector shown in Fig. 1, we have adjusted the timing deviations between the four signal-

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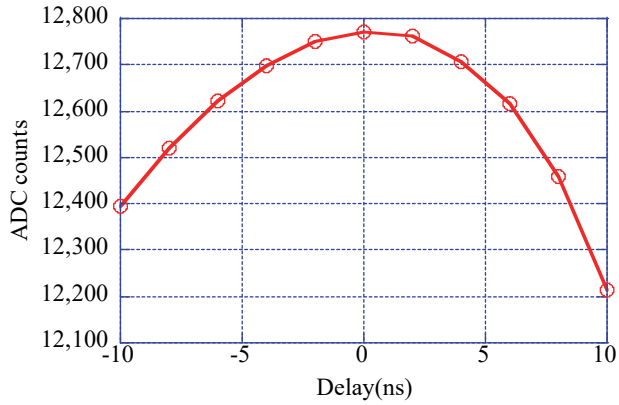

Figure 1: Pulse response of 18K11 L/R detector.

cables from the BPM feedthrough to 18K11s less than few mm by the cable length adjustment using TDR function of Agilent E5071C Network Analyzer. While the timing deviation before the adjustment distributed from 1 to 5 cm on the typical cable length of around 30 m, the final deviation was 30 ps in standard deviation. It is also clear that it is needed to control the ADC timing within 4 ns for each 18K11 to guarantee good response.

Though the data transfer speed from 18K11s to VME IOC (MVME5500) has been increased by using 64bit DMA transfer [2], it still needs more than 3 seconds to process 10 or 11 18K11 cards (transfer 32k turns of data to CPU, calculate the beam position using 3rd order polynomial fit using data from the mapping data) due to low CPU power. The start trigger is needed to be disabled during the data transfer and calculation to avoid re-triggering the modules that have finished the data processing.

DR BPM TIMING SYSTEM

Figure 2 shows the block diagram of the timing system for DR. It consists of mainly three parts; start trigger generation system, frequency divider with external synchronizer, and 32-channel clock delay per each station.

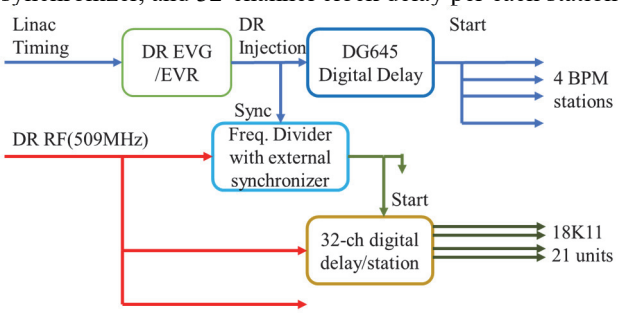

Figure 2: Block diagram of DR BPM timing system.

Start Trigger Timing Generation

In the normal operation, we want to get the position data in the similar timing slot, starting with the same delay after the injection. The start-trigger is also needed to be disabled during the processing time of the beam position monitor system. On the other hand, manual or continuously repeating trigger will be needed during the long storage timing mainly on the machine development time.

To realize the requirements, we have constructed a start trigger generation system using digital delay with external trigger (SRS DG645) [3] controlled by EPICS software sequencer. We have prepared three operation modes as:

- Normal operation mode. If the status of the end node of 18K11 is ready, the sequencer enables the single shot external trigger input. Start trigger (Single Shot pulse) is initiated by the injection timing signal with pre-set delay. EPICS sequencer waits for the ready status of 18K11 and automatically re-initiate the trigger.
- Storage mode. It is similar to the normal mode but start trigger is periodically initiated by the software timing without injection timing.
- Manual mode. Start trigger is controlled by the software. The mode will be used mainly on the special optics measurements such as dispersion measurement or chromaticity measurement where optics tool will govern all the measurement timing.

We have tested the start trigger system with the storage mode more than 6 months and had no difficulties up to now. Typical cycling time of the measurement is about 4 s where we have inserted extra 1 second of sleeping time of data acquisition to enable enough communication timing for EPICS channel access.

Frequency Divider with External Synchronization Timing

As the injection timing signal supplied by the linac / DR event system has enough precision with the typical timing jitter less than 10 ps, we generate the DR revolution timing synchronized to a injected bucket by re-synchronizing the frequency divider (1/230) with the injection timing. We have developed a 32-bit universal frequency divider with 32-bit clock delay and re-synchronized function (SKI-16115). Figure 3 shows the block diagram of SKI-16115.

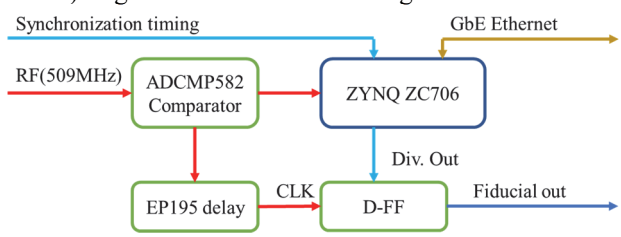

Figure 3: Block diagram of SKI-16115 universal frequency divider.

It consists of a Xilinx ZC706 evaluation board and a daughter card connected with FMC connector and installed in an EIA-1U case. All the functions of the board such as the set/read the frequency divide ratio, digital delay setting, enable/disable external synchronization, EP195 delay are accessible from a EPICS Soft-IOC through socket communication controlled by the Peta-Linux on the ZYNC FPGA.

The timing deviation and the timing jitter with the delay (RF and EPE195) change at the frequency division ratio of

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230 has been measured using histogram function of Tektronix DSA8200 with 80E07 (30 GHz BW) module. Figure 4 shows the photo of the setup of the jitter measurement. The measured results are shown in Fig. 5, where the peak to peak deviation was about 4 ps with the flat timing jitter of less than 2.6 ps in all delay setting. By the comparison with the RTD temperature sensor near SKI-16115 and DSA8200, the change of the mean position

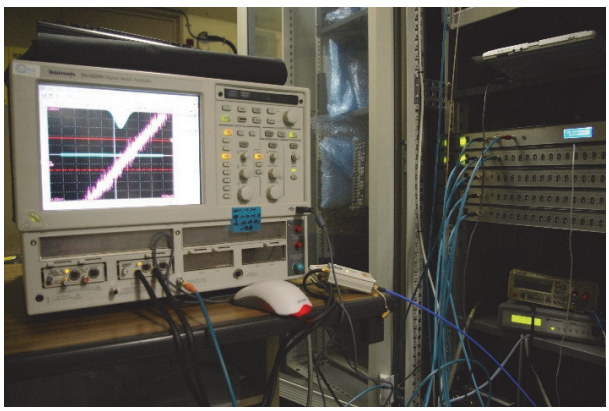

Figure 4: Photo of the jitter measurement setup.

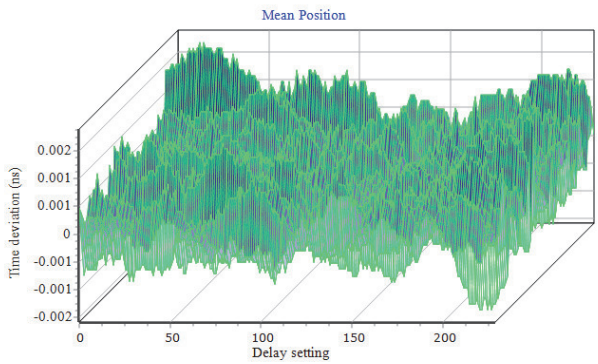

Figure 5: Measured timing jitter of frequency divider. Traces on depth axis correspond to delay for EP195 from 0 to 2 ns with 100 ps step.

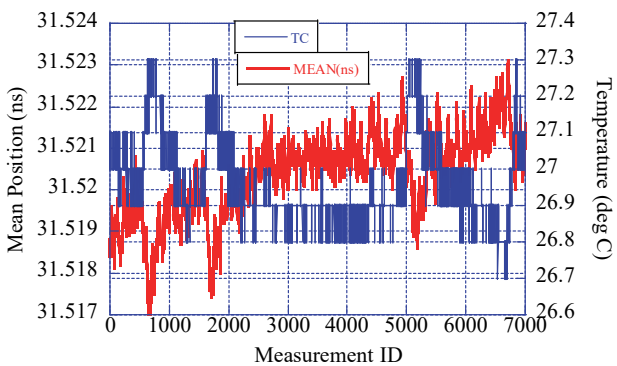

Figure 6: Temperature dependence of the output.

shows clear correlation, roughly 2ps / 0.4 deg. C as shown in Fig. 6.

As the design and the resources needed for the frequency divider has been established with this system, we are fabricating the new board with the same functions by employing smaller ZYNC FPGA (702) with the final form factor of NIM 1W.

32-Channel Digital Delay

From the measured cable length and the BPM location in the ring, the fiducial timing delays for each 18K11 module have been calculated relative to the latest signal in a BPM station. Though the ring size is not large, the largest delay for two stations amounts to more than 180 ns. As it is not suitable to prepare such long delay with the change of cable length, we have decided to develop a 32-channel 32-bit digital delays (SKI-17029) also with the form factor of EIA-1U based on the code for SKI-16115 which counts RF clock (509 MHz) starting with the external timing (coming from SKI-16115) and distributes the fiducial timing for each 18K11 with the arbitrary delay with step of 2 ns. It consists of a Xilinx ZC702 evaluation board with a daughter card which has a RF comparator, 32 D-FFs and the level shifters from LVDS to PECL and PECL to NIM as shown in Fig. 7.

Figure 7: Photo of the 32-channel digital delay (SKI-17029).

Figure 8 shows the measured timing deviations and its standard deviation of jitter using the similar setup as that for frequency divider with the external fiducial input from SKI-16115 (div=230).

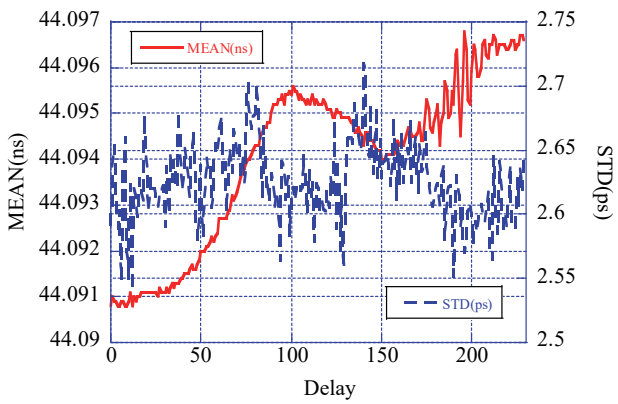

Figure 8. Measured timing jitter (mean position: red solid line, standard deviation: blue dashed line) of 32-channel delay (SKI-17029).

The change of the mean position also has clear correlation with the change of the environment temperature

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and has no correlation with the temperature of the SKI-17029 (around 40 deg. C on the top of the box). It is therefore the temperature dependence of the DSA8200 system is supposed to be the main source of the mean position change. Of course, unexpected very high temperature of SKI-17029 needs to be decreased for safer operation. Presumably due to so tight space in the box with so many PECL ICs and so large resources in the FPGA, the temperature of SKI-17029 reaches more than 50 deg. C in the box. Though the 32-channel. delay is working without trouble more than a week with this temperature, we are planning to add cooling fans with improved air conductance to reduce the temperature. If the leakage of the RF signal from this module is small enough not to affect the 18K11 modules in the same rack, we might open the top panel for better cooling. The EPICS (asyn) device support based on the socket communication protocol has been developed and tested and confirmed to be working.

SUMMARY

We have constructed the timing systems for the SuperKEKB DR beam position monitor systems. The start trigger system generates the data acquisition start signal synchronized to the beam injection timing with output veto not to disturb the data transfer and data processing.

The 32-bit universal frequency divider with 32-bit delay (SKI-16115) generates the master fiducial timing also synchronized to the fine injection timing. The time deviation and jitter due to the change of delay has been measured to be small enough.

To provide the individual ADC timing to 18K11 detectors in the BPM station, 32-channel, 32-bit digital delay (SKI-17029) has been developed using the resource of SKI-16115. The time deviation and jitter due to the change of the delay has also measured and confirmed to be small enough. The unexpected higher temperature of SKI-17029 needs to be solved soon.

Both SKI-16115 and SKI-17029 use the ZYNC FPGA with ARM core inside. Up to now, we have installed embedded Linux system on the FPGA (Peta-Linux) and controlled the function through GbE Ethernet. After the initial setting just after the first beam storage, it might be fairly rare to change the parameters such as individual delay. Therefore, we do not have strong motivation to optimize the communication, such as the tuning in the communication buffer, to increase the data transfer or to reduce communication error with very crowded condition. Nevertheless, we are trying to install EPICS system on the FPGA which should have enough computing resources. Working without external server should be preferable especially for the new universal frequency divider with NIM form factor.

The authors would like to thank our colleague of SuperKEKB beam instrumentation group for numerous supports on the development and construction. Discussion with the control / timing group of Linac and ring are so fruitful.

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