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DESIGN OF A NEW TYPE OF BEAM CHARGE MONITOR BASED BUNCH BY BUNCH DAQ SYSTEM *

F. Z. Chen , L. W. Lai†, Y. B. Yan, Y. B. Leng
SSRF, SINAP, Shanghai, China

Abstract

Beam current is one of the fundamental parameters to be measured in storage ring. The Shanghai Synchrotron Radiation Facility (SSRF), a third generation light source with the RF frequency of 499.68 MHz, used adopt commercial product to monitor beam charge. However, the maintain and upgrade is not always straightforward. Thus, a new type of beam charge monitor (BCM) based on beam positon monitor (BPM) sum signals has been developed for the online beam current measurement on SSRF storage ring. This system has been convincingly validated by mathematical analysis, and has been demonstrated with beam experiments during machine study time.

INTRODUCTION

We used to employ the commercially BCM manufactured by Acqiris, however, the maintain and upgrade is not always straightforward. In the electron accelerator, the beam position detector can be used to measure beam charge. Since BPM sum signals provide a new type of solution of beam charge monitor in SSRF, and there're 140 BPMs in the storage ring, we choose the one meet the criteria for this particular usage under particular measurement [1]. For data acquisition system, obviously, the higher the sampling rate, the more precise the original signal reconstruction. However, consider of the sampling rate measurement accuracy and equipment cost, we choose sample rate at RF frequency.

The DBPM processor system played a vital role in beam diagnostics system. The BI group of SSRF developed a new type of DBPM processor to handle the BPM data acquisitions and the position calculations. The BPM processor carry FPGA and ARM, available for further application development. The processor also could use external trigger and external clock. Under the circumstances, we design a new type of BCM based on BPM sum signals using the DBPM processor, namely, a DBPM-BCM. .We design a new type of BCM based on BPM sum signals using a new type of BCM

The DBPM-BCM consist of three parts: pick up, front-end electronics and the data acquisition. In order to monitor beam charge bunch by bunch, consider of DBPM external clock sampling rate, we divide the storage ring bunches into four parts. Using delay line to generate RF frequency interval, make the sum signal reach 4 channels at different interval, in our system which is a 2 ns interval one after one. This design of signal transmission guarantee each channel acquire a different quarter of bunch cluster in storage ring. Adjusting the sampling clock phase to acquire signals peak value is the core requirement of the system, and has a profound effect on the measurement accuracy and reliability. Therefore, the sampling phase must be cautious adjust. Another one of the key challenges of the system is to find a suitable sample frequency, and delay the signals to ensure every single bunch in the storage ring should be captured. The transmission phase also needs to be cautiously adjusted.

The main reason why the bunch-by-bunch separation sample method chosen is that independent test can extract the irrelevant four bunch clusters in storage ring. This feature assures every single bunch in the storage ring has been monitored. The total design is neat and obvious. That makes the method easy to be implemented and work online.

*Work supported by National Natural Science Foundation of China (No.11575282No.11305253)
†lailongwei@sinap.ac.cn

DESIGN AND REALIZATION OF THE SYSTEM

System Requirements Analysis

Take full use of the existing beam diagnostic equipment in the storage ring, establish a set of bunch-by-bunch BCM data acquisition system (DAQ) system, given the current intensity information of each bunch, the measurement accuracy should meet the top-up actual operational indicators.

DBPM has a 16-bit resolution, DC-700 MHz bandwidth baseband data acquisition card, which meets our present needs. The electron accelerator could provide accuracy RF frequency demultiplication, and in our system it should be a quarter of RF frequency used for external sample clock.

The Principle of BCM

According to model building and formula proving, the relationship between the average beam current and four electrode sum signals can be expressed by Eq. (1):

$$I_{avg} = \frac{k(x,y)*V_{sum}}{Z} \qquad (1)$$

Where the Z is the equivalent impedance constitute detection electrode and the signal transmission network, k(x,y) is the current intensity correction factor dependent on beam position, V_{sum} is detect electrode output sum signal voltage [2]. Using the button electrode BPM and the sum signal pulse measure pulse current intensity. The equation also suit for beam charge monitor.

When the ADC sample rate could reach RF frequency, we can realize bunch-by-bunch beam charge monitor. The criteria are the following: use four channels of DBPM processor to acquire sum signals, each channel has a 2 ns

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delay compare to ahead channel, and we set the external sample clock a quarter of RF frequency.

A central element of the system is capturing the peak phase signal. In order to realize the high precision measurement of bunch-by-bunch beam charge monitor, we design the system based on accuracy phase positon regulate.

The architecture of the system is described below. A high-level overview is provided of the hardware, embedded software and control system (Fig. 1).

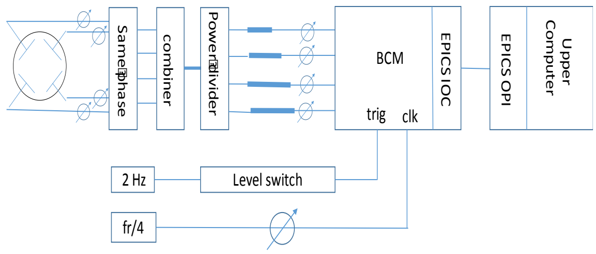

Figure 1: The overview architecture of BCW test system.

The beam charge monitor in the SSRF storage ring represent this new design and satisfy the high precision measurement of the top-up current injection mode.

Hardware Design

Four channels of RF signal extract from the button BPM electrode, signals transmit to synthesizer through the coaxial cable, using adjustable phase shifter to keep four channel signals in-phase, the combiner take signals four in one. Then, using power divider divide the sum signal into four channels. The delay line and phase shifter control the signals reach time difference.

The phase control system consists of three main components: signal extract port need phase shifters to make sure four channels in-phase; sum signal divide to four channel to provide four bunch clusters, and the phase shifter works on external clock to help sample at signals peak value.

The design takes fully use of the hardware facility of SSRF and turns out to be a cost-effective solution.

ADC sampling clock from the storage ring high frequency clock, to ensure that ADC sample are synchronization with bunch-by-bunch data to avoid phase slide.

Software Design

The architecture of the entire system software is based on the EPICS and Linux environments. Upper software control data acquisition card. The DBPM-BCM embedded EPICS IOCs, running Linux operation system. The soft IOC has good real-time performance, portability and extensibility. DBPM-BCM IOC collects data from four channels. The EDM panel consists of two main parts: one is display windows showing readouts acquired through EPICS IOCs, and the other is parameter setting. We set the sample external clock and external trigger using the EDM panel.

MATLAB gets PVs from DBPM-BCW processor via labCA, which is an EPICS channel access interface for MATLAB developed by SLAC. We designed a dedicated algorithm to realize four channels split joint.

LABORATORY TEST

Test Platform

The test system has already set up in the laboratory as the photo shown below. The platform followed the principal of compact. Both of the sum signals and timing signals come from accelarator provide by a equipment cabinet.

Figure 2: Photo of platform in laboratory.

Test Results

The test system get four channels raw ADC data simultaneously from the DBPM processor, each channel get a train of storage bunch cluster. Figure 3 below is the independence test, which could prove four channels acquire a different bunch cluster. Considering the limitation of bandwidth and crosstalk, the independence test showing the different channels are not completely irrelevant variables.

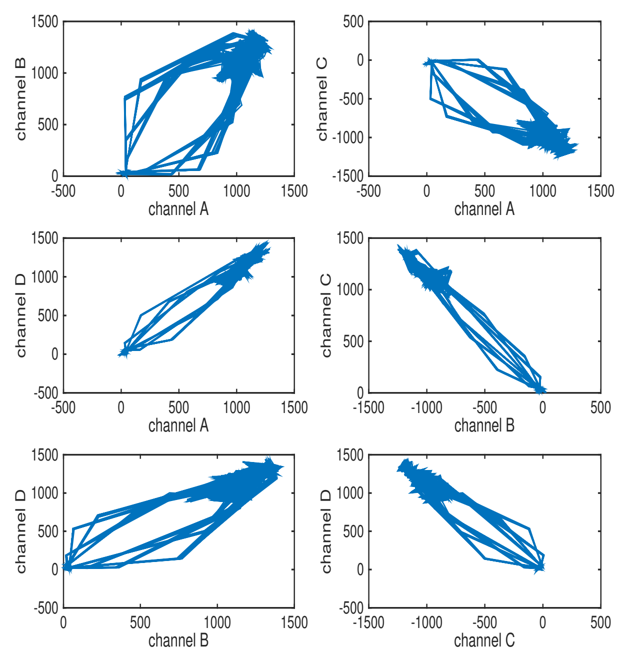

Figure 3: Independence test of each channel.

We could optimize the system in the future. Therefore, the four channels could split joint the complete storage beam charge, which is also shown below in Fig. 4.

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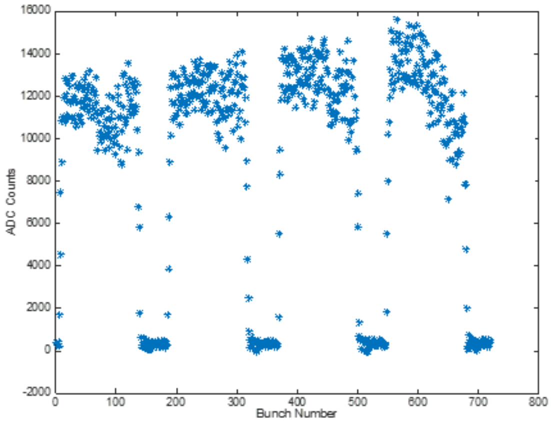

Figure 4: BCM of the storage ring.

Calibration Algorithm for Bunch-by-Bunch Current Intensity

The sampled value obtained by ADC sampling is not real bunch-by-bunch current intensity, but there is a certain proportional relationship between the value and the real current intensity. In addition, the current intensity of the bunch could be obtained by calibration. The calibration factor K can be calculated using the following formula:

$$K = \frac{I_{DCCT}}{(f_{rf}/720)} / sum(Q) \quad (2)$$

I_{DCCT} is the mean current of the circulating beam, measured by parametric DC current transformer (DCCT), which measures average beam current, but not capable of measuring the charge of an individual bunch. The frequency of RF is also read by EPICS PVs in real time. So the numerator is the total current intensity in the storage ring. The denominator is the sum of the signals sampled by the ADC, where the Q is the ADC readouts. In the process, each time the calculation requires the reading of the DCCT to calculate the new calibration factor. Current intensity calibration coefficient is difficult to accurately calculate or calibrate off-line, must through the beam experiment and other current intensity detector (such as DCCT) for on-line calibration.

CONCLUSION AND OUTLOOK

The BPM sum signal has been used as an alternative to beam charge monitor in SSRF storage ring. The paper has shown the DBPM-BCW bunch-by-bunch DAQ test system in terms of hardware, firmware and software. Its complete integration into the EPICS based control system allows other extension applications, which could be further development.

The current can be simply the useful quantity in itself, but often it is an intermediary for measuring beam lifetime or for machine safety systems in storage ring. Because of the flexibility of this system, we can develop other applications based on FPGA, such as the beam lifetime analysis in the electron storage ring, providing more details of beam charge measurements during operation. We plan one of the upgrades is beam lifetime calculation application.

Finally, this system still exist many problems, such as the phase slide, which could be arisen by signal transmission and other kinds of random error. In terms of resolution and stability, there is a demand to improve the performance and optimize the algorithm. We can use FPGA algorithm to realize waveform reconstruction, in that way, the system could be more stabilization.

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