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HIGH-SPEED BEAM SIGNAL PROCESSOR FOR SHINE *

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Abstract

A CW hard X-ray FEL is under construction in SSRF, which pulse rate is designed to 1MHz. A new high-speed sampling BPM signal processor is under development to meet the high performance requirements of beam position measurement system. The processor's sampling rate can be up to 500MHz, and beam position information of each bunch (1MHz rate) can be retrieved with the power of FPGA. Time stamp is aligned with the position data for offline analysis. The processor is designed to be a common signal processing platform for beam diagnostics. The first application is cavity BPM, and other applications, including button BPM, stripline BPM, and even wire scanner processor will be developed based on this platform. At the same time, a RF direct sampling processor is designed for cavity BPM signal processing. This novel technology will greatly simplify the cavity BPM electronic system, and make the system design more efficient and more flexible.

INTRODUCTION

SHINE is the abbreviation of Shanghai HIgh repetition rate XFEL aNd Extreme light facility. SHINE is a 3110 meters long accelerator locates at the 29 meters deep underground near SSRF. The energy is designed to be 8 GeV and repetition rate up to 1MHz. SHINE composed of a LINAC and 3 undulator lines, and to be completed in 2025.

There will have more than 300 cavity BPMs, stripline BPMs and button BPMs distributed along the injector, LINAC and undulator. A general BPM signal processing platform(DAQ) is under development to meet the diverse BPM data acquisition and signal processing requirements. RF conditioning components locate in an independent module before the DAQ.

The DAQ will apply state-of-the-art technology today to ensure the high performance even after 2025. Including a powerful SoC FPGA and high sampling rate and high resolution ADC. DAQ will supply 1MHz rate bunch position data with aligned timing information.

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PROCESSOR STRUCTURE

The DAQ is designed to be a SoC FPGA based standalon instrument. Figure 1 shows the DAQ structure. A Xilinx Zynq SoC FPGA containing both Arm CPU and FPGA, which enables realtime signal processing, data transfer and system control on one chip. The FPGA makes the DAQ structure simple and stable. There have two FMC interfaces on the FPGA board supporting two FMC cards for special applications. One is ADC FMC card for analoge signal digitizing. One is white rabbit FMC timing card providing timing information for each trigger. Besides are peripherial components such as DDR, connectors and indicators.

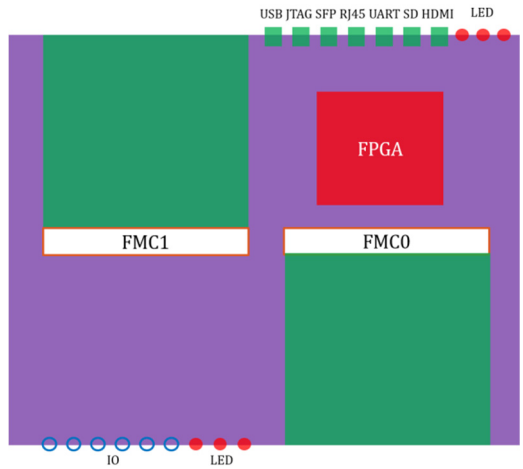

Figure 1: DBPM signal processing structure.

DAQ is desined to be 1U height. Figure 2 is the chassis size and the front panel and back panel. There have various connectors on the front panel, such as timing FMC card slot, JTAG, SFPx2, RJ45, UART, SD card slot, I/O, USB. Back panel have an ADC FMC card solt, and some IO connectors.

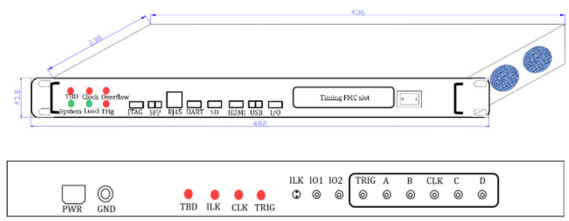

Figure 2: DAQ front and back panel.

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IF SAMPLING ADC FMC CARDS

Currently, most of the digital BPM signal processor sampling at about 100 MSPS. These are high performance ADCs at 10 ago. However, more ADCs sampling speed higher than 500MSPS are appeared. Higher digitizing speed introduces better signal processing performance. There is no doubt that they will be the main ADCs on BPM processors for the foreseeable future. The DAQ for SHINE will apply ADC sampling at 500MSPS (or 1GSPS) and resolution ≥12 bits.

This 4 channels IF sampling ADC card (AC version and DC version) can meet most beam signal processing requirements on SHINE, also can be used for bunch-by-bunch signal processing on SSRF storage ring.

DIRECT RF SAMPLING ADC FMC CARD

Bandwidth, sampling rate and resolution are three important parameters for ADC. With the development of semiconductor technology, direct RF sampling ADCs come into production. There have some ADCs that bandwidth high than 5GHz (or up to 9GHz) that can be used to sample the C band cavity BPM signal directly.

Currently, superheterodyne receiver structure is used for cavity BPM signal processing. There have complex down conversion RF modules before ADCs, such as LO, mixer, filters. RF modules make the system complex, brings noise and unstable factors. Cavity BPM on SHINE is designed to be C band. The narrow bandwidth signal from cavity BPM makes it quite suitable for direct RF sampling [1]. Figure 3 comes from Xilinx, this is a system structure comparison between IF superheterodyne receiver and direct RF-sampling receiver. Obviously, the structure is highly simplified after applying direct RF-sampling ADC.

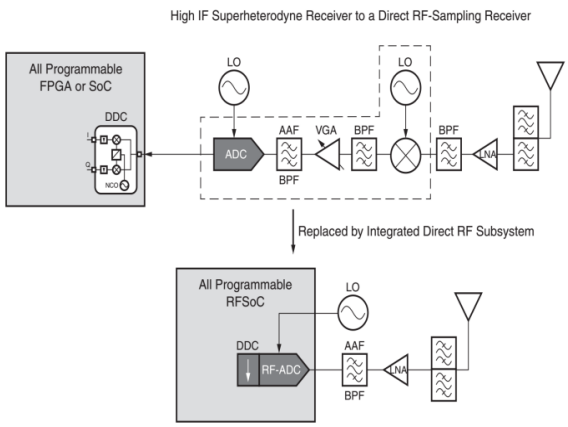

Figure 3: Comparison between superheterodyne receiver and direct RF-sampling receiver.

A direct RF-sampling ADC FMC card will be designed to explore the possibility of application on cavity BPM signal processing on SHINE. Once the production is possible, the cavity BPM system structure will be much simpler, more stable and more flexible. It will be a significant progress for the beam instrument.

TIMING FMC CARD

There is a FMC slot for Whit Rabbit Timing card on DAQ. WRT is an Ethernet based synchronization protocol. White Rabbit provides sub-nanosecond accuracy and picoseconds precision of synchronization for large distributed systems [2]. It provides high precision timing information for each node. Each DAQ will support the FMC interface and decoding module. The decoded timing information will be used to synchronize all the BPMs data along the SHINE. This is really useful for commission, control and machine study.

FPGA PLATFORM

Xilinx Zynq Ultrascale+MPSoC ZCU102 Evaluation Kit is used for development [3]. This is a powerful board with large-scale resources and rich interfaces that meet the DAQ requirements quite well. We can deploy DAQ firmware and software on the board at early stage and move to designed board later. And the open source PCB design can be used to design the DAQ hardware.

Figure 4 is the hardware picture. An evaluation DAQ kit will be designed with ZCU102, a FMC ADC card and a FMC timing card.

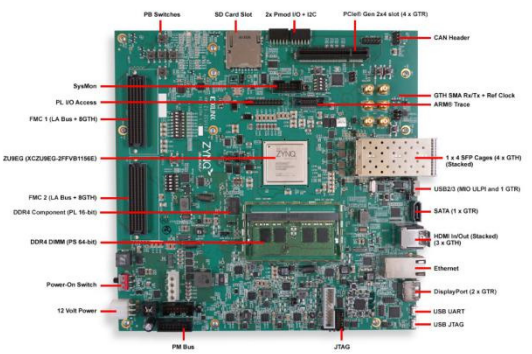

Figure 4: ZCU102 evaluation kit.

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