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ESS BEAM POSITION AND PHASE MONITOR SYSTEM

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Abstract

The European Spallation Source (ESS) is a neutron facility under construction in Lund, Sweden, and established as a European collaboration between different member countries. The machine is a 2 GeV proton LINAC with a nominal beam current of 62.5 mA, 2.86 ms of pulse length and a bunch repetition rate of 352 MHz. The Beam Position and Phase Monitors (BPM) at ESS were designed to satisfy the specifications for the different beam modes, which span from 5 µs pulse length and 6.3 mA beam until the nominal beam condition. The system is designed for standard beam position measurements for beam trajectory correction and for beam phase measurements for cavity phase tuning, imposing restrictions on the sensor design and electronics architecture. Approximately a hundred BPM's were manufactured and are being installed by partners in collaboration with ESS. The BPM system comprises a MicroTCA.4 electronics based in COTS AMC and RTM modules with custom FPGA firmware implementation and a custom Front-End electronics. In this work, the system architecture, implementation, and test results are presented and discussed.

INTRODUCTION

The ESS beam position monitor system is an RF receiver system based on a superheterodyne architecture with high speed IF sampling designed for improved RF phase measurements.

Table 1: ESS BPM system specifications. The precision numbers are provided with the bandwidth specified in the table.

Parameter	Value
Phase precision for nominal beam	0.2 °
Phase accuracy for 6.3 mA beam / 5 us pulse length	+/- 2 °
Phase precision for 6.3 mA beam / 5 us pulse length	2 °
Phase stability over 8 hours for nominal beam	+/- 1°
Beam position precision for nominal beam	20 um
Position accuracy at 6.3 mA / 5 us pulse length	+/- 400 um
Position precision at 6.3 mA / 5 us pulse length	200 um
Position accuracy stability over 8 hours	1 mm
Phase and Position bandwidth	1 MHz

The ESS BPM system is composed by approximately 100 BPM stripline and button BPM sensors which were designed in a collaboration between ESS beam diagnostics team and collaborations across several European institutes.

RF phase measurements are most stringent than amplitude measurements in the ESS BPM system and a phase stable reference line is distributed along the accelerator for both BPM and LLRF systems. The RF phase of the signals excited to the BPM sensors are compared to the phase of the reference line to provide the user with phase measurements on each BPM relative to the phase of the reference line. The specifications for the ESS BPM system is shown on Table 1.

ESS BPM System Architecture

The BPM signals are transmitted through cables ranging from 20-80 meters, from the sensor to the electronics, and are bundled together along its extension with the reference RF cables. The receiver channels are digitized separately and phase and amplitudes are measured independently in the digital domain. Comparison of the digitized phase and amplitudes are performed in the FPGA firmware to provide the user with beam X and Y positions and relative phases between BPM sensor inputs and the reference signal.

Near-IQ is used on the BPM receiver with an IF/CLK ratio of 4/15 providing a bandwidth of approximately 11.7 MHz around the IF without having nonlinear higher order frequency components lying within the first Nyquist zone of the digitized signal [1].

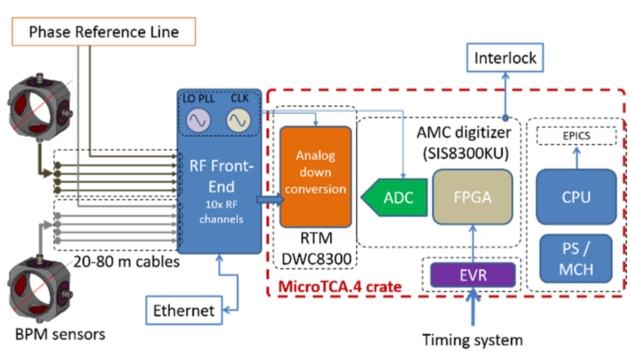

Figure 1: BPM system block diagram.

Every pair of BPM sensors are digitized in the same digitizer board as shown in Fig. 1, allowing strong noise correlation between channels and also improved relative thermal drifts between pairs of BPM's. The ESS BPM

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system measures the phase of each individual BPM, however for each pair of BPM sensors, this phase difference is measured in a single FPGA and can be used for low latency fast interlocks in future expansions of the system.

BPM SENSORS

Four different types of BPM sensors were designed for the ESS project. At the low beta part of the LINAC (MEBT and DTL), stripline BPM sensors are used and at the high energy part of the LINAC, button BPMs are used, as shown in Fig. 2.

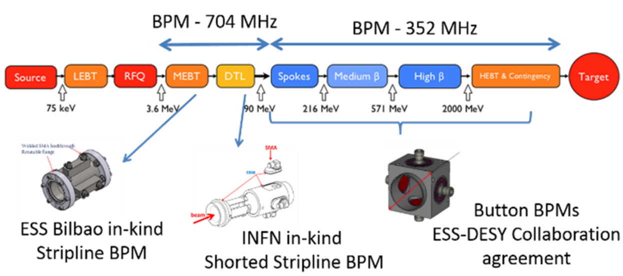

Figure 2: BPM sensors for the ESS LINAC.

Stripline BPM's for MEBT are embedded into the quadrupoles and the mechanical and electromagnetic design is constrained to fit inside the quadrupole geometry. BPM response is designed to work at the second harmonics (704 MHz) and the striplines are terminated with SMA feedthroughs in both ends, allowing it to be left open, shorted or matched with a 50 Ohms load [2].

Beam tests have been performed at CEA Saclay IPHI accelerator to evaluate the MEBT BPM response at 3 MeV and across several different beam modes. Current sweep tests were performed from 0.4 mA up to 50 mA and the pulse length was changed from 150 us up to 3 ms.

DTL BPM's are shorted striplines and are constructed inside the drift tubes. Short cables connect the sensor to the patch panel. Coaxial Kapton cables were chosen for this application to avoid long term radiation issues with the dielectric despite having a phase dependence in the order of 0.1° / °C at 704 MHz. Non-PTFE connector dielectrics are chosen for the short patch cables and connectors to avoid radiation damage of the materials in the long term [3].

For the high energy part of the LINAC, two different sizes of buttons were designed where a BPM body with different chamber diameter can be used. Button BPM's were chosen for the high energy part of the machine due to its simpler construction, lower cost, as well as a design capable of providing enough signal across all the beam modes. The BPM's are composed of the N-type feedthrough with a glass-ceramics insulator (BC-Tech, Switzerland) which are welded into the BPM body. The whole BPM is welded into the vacuum pipes, as Fig. 3 shows.

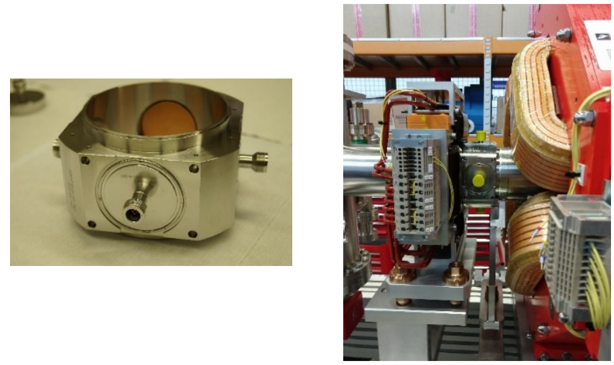

Figure 3: Linac Warm Unit BPM before and after welding into the vacuum chamber.

Since the machine duty cycle is in the order of 4%, thermal simulation showed that the expected heat dissipated on the BPM due to first trapped mode is in the order of 5 mW [4].

Short heliax patch cables with Polyethylene dielectric are going to be used to connect the N-type connectors from the BPM sensor to the long cables. Majority of the BPM's are welded into the vacuum pipe however in some locations they are flanged due to its simpler maintenance.

BPM ELECTRONICS

ESS has adopted the MicroTCA.4 platform for high speed data acquisition systems as a standard across the accelerator. BPM electronics was designed based on COTS Advanced Mezzanine Card (AMC) data acquisition platform SIS8300-KU (Struck, Hamburg, Germany) and the 10 input analog down convertion Rear Transition Module (RTM) DWC8300.

An analog front-end electronics is used to perform analog processing of the signals at the RF frequency. The RTM is responsible for the analog down conversion stage using a passive LO signal distribution to provide phase noise correlation of the LO signal among different channels.

The phase reference line is a rigid coax transmission line filled with nitrogen dielectric for better temperature stability and low RF phase drifts. RF couplers and splitters are used to distribute the RF signal along the LINAC and are also temperature stabilized [5].

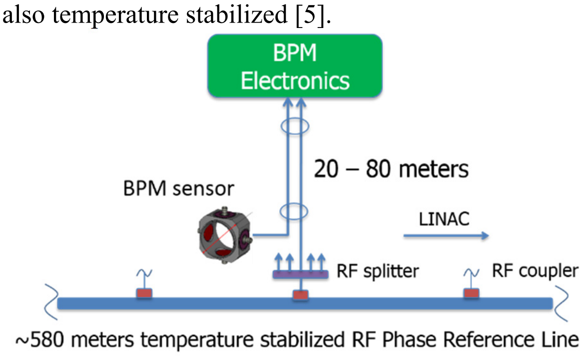

Figure 4: Schematic scheme of BPM cables bundled with phase reference line cables.

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The phase reference line RF signal phase accuracy stability is 0.1 ° at 704 MHz in the long term between 2 adjacent outputs. The RF phase reference line and the BPM signal cables are bundled together very close to the BPM sensor and are pulled together until they are connected to the Front-end electronics, as Fig. 4 shows.

Several different cables with different dielectrics have been tested to determine the materials and cable models which were more stable as function of the temperature. Temperature dependence tests were performed inside a climatic chamber in a temperature controlled environment.

Heliax cables have been selected due to their particular stability over temperature drifts within +-0.02 ° of RF phase at 352 MHz and 704 MHz (1st and 2nd RF harmonics) for temperature variations smaller than ~5 °C. Temperature of the test was changed from 10 °C to 65 °C in 5 °C steps of 2 hours and 2x 40 meter cables were used inside the climatic chamber. Cables are also purchased from the manufacturer after a thermal annealing process is performed. 4-port VNA was used for the measurements and kept at ambient temperature. The phase difference between the cables were compared.

Since the BPM acquisition system is sensitive to cable length differences between the channels of the same BPM, a length matching procedure is done to match the length of the 4 cables of each BPM to the same length.

RF Front-End Electronics

The front-end electronics of the ESS BPM system provides 3 cascaded 20 dB gain stages which are followed by digitally controlled attenuators and AC coupled RF filtering stages. Fig. 5 shows the RF chain and a picture of the PCB.

The front-end unit has 10 RF channels with 2 of them being used for the reference line inputs and 8 channels are used for 2 BPM's. The center frequency of the RF channel can be configured for the first or the second RF harmonics by changing the RF bandpass filter. Several narrowband RF bandpass filters technologies have been tested to evaluate its amplitude and phase response as function of temperature. Wideband, 100 MHz bandwidth, discrete passive RF bandpass filters (Mini-circuits, EUA), narrowband, 20 MHz bandwidth, ceramic filters (Filtronetics, Kansas city, EUA) and narrowband 20 MHz bandwidth helical filters (Temwell, Taipei City, Taiwan) were tested over a range of +-5 °C at 704 MHz where amplitude and phase were monitored over several hours. Narrowband ceramic bandpass filters were chosen for the final production due to its lower temperature dependence.

The LO signal is generated inside the Front-end electronics by the use of a low-phase noise PLL (LMX2582). ADC signal clock is also generated in the Front-end electronics by the use of low additive phase noise frequency divider IC (AD9515) and it's then distributed to the RTM clock input which drives the high speed ADC's in the AMC boards.

Ethernet interface is embedded into the front-end electronics by the use of a COTS Ethernet to serial module (AK-nord, Germany) with isolated power supply and communication data lines. Attenuators are controlled through serial interface of clock, data and latch lines.

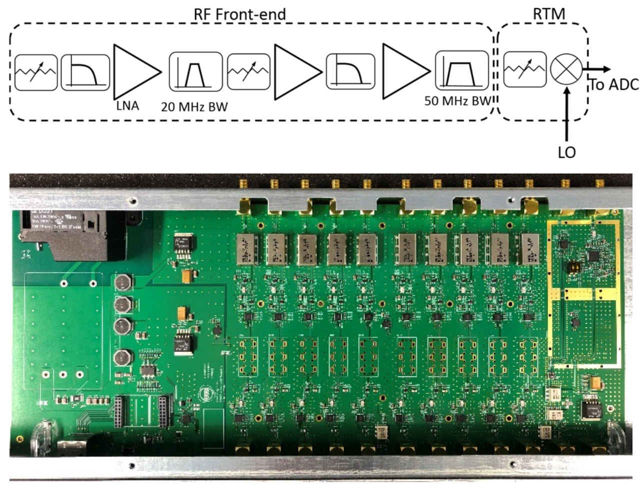

Figure 5: Front-end electronics RF chain and PCB. Bandpass filters are not shown in the picture.

A low insertion loss attenuator is placed on the input of the RF chain, just after an impedance matching generic circuit, to avoid nonlinearities to be excited on the chain for some beam modes expected at ESS. A low noise figure input amplifier keeps the whole RF chain noise figure low when low input power signals are excited on the inputs of the receiver.

MicroTCA.4 Data Acquisition Hardware

The SIS8300-KU AMC hardware has 10 ADC channels capable of sampling at a rate of 125 MSPs per channel. The RTM can be configured during manufacturing to operate with 352 MHz or 704 MHz input frequency range.

Figure 6: AMC and RTM boards for BPM system.

Each pair AMC and RTM board is able to measure the signals from 2 BPM's, allowing a strong correlation of the high frequency noise from LO and ADC clock signals and also a strong correlation of the long term drifts. The thermal stabilization of all the RF channels is performed by the bottom and top aluminium shielding cover. The RTM and AMC boards are shown together in Fig. 6.

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FPGA Firmware

BPM firmware has been designed in a collaboration with LLRF implementation and it performs separated channels digitalization, baseband conversion and amplitude and phase measurements. After each channel amplitude and phase is obtained from the cartesian to polar coordinates conversion, position and BPM phase is obtained. For phase measurements, the 4 antennas of each BPM are summed and then compared to the phase of the reference line. The FPGA firmware block diagram of Fig. 7 shows the firmware architecture. User has access to ADC raw data, baseband amplitudes and phases of all channels, sum signal of the amplitudes of the 4 inputs per BPM, beam position and averaged value along the pulse by selecting a window of interest.

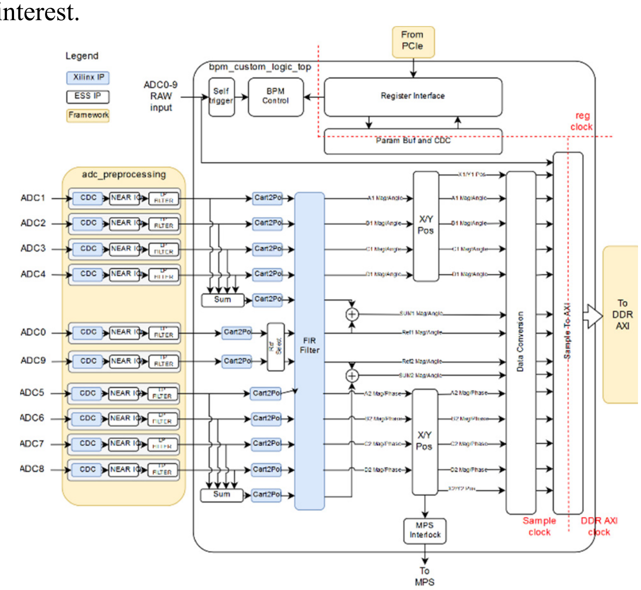

Figure 7: FPGA firmware diagram.

Electronics Performance Evaluation

The BPM electronics has been tested using low phase noise RF generators exciting the RF inputs and generating the RF reference to the PLL circuit and ADC clock divider circuit. RF splitters were used to split the signal to the RF inputs and the reference inputs. An EPICS IOC was developed to monitor all the Process Variables of the raw data, baseband individual channels amplitudes and phases, BPM phases and positions.

The phase resolution as function of the input power for an acquisition bandwidth of 1 MHz has been measured and is shown in Fig. 8. Integrated RMS noise is also shown in Fig. 9 and Fig. 10. Long term tests have also been performed to assess the performance of the whole system as function of temperature. It has been measured a drift performance between pairs of BPM's of less than 0.05 ° of RF phase variation at 704 MHz, when temperature variations of 5 °C are forced to happen in less than 15 minutes, which exceeds the requirements for ESS phase measurements.

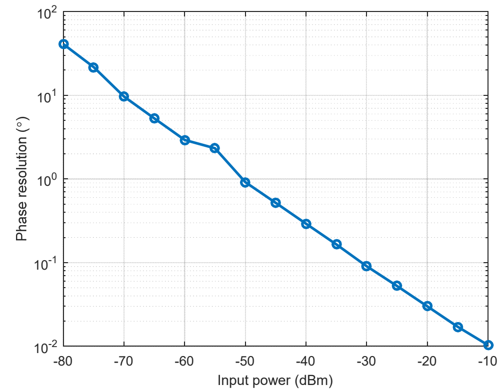

Figure 8: Phase resolution as function of the input power in a 1 MHz bandwidth.

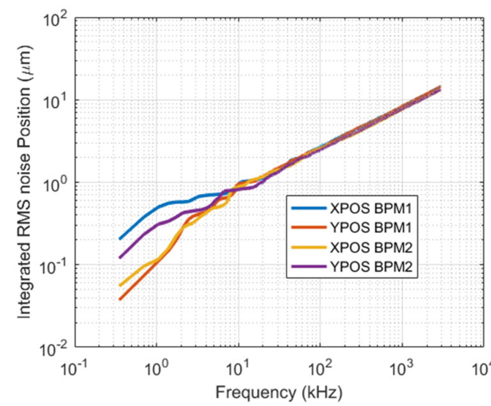

Figure 9: Integrated RMS position noise for a 3 ms acquired pulse and -30 dBm input power.

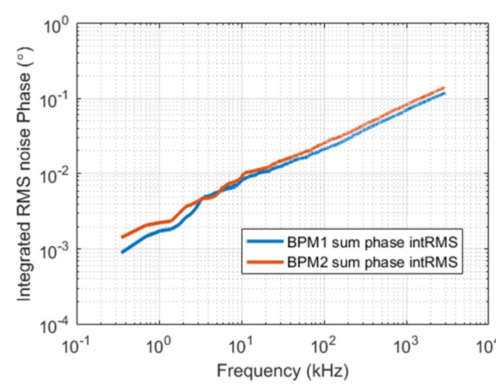

Figure 10: Integrated RMS noise phase for a 3 ms acquired pulse and -30 dBm input power.

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