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BPM SYSTEM FOR THE PIP-II INJECTOR TEST FACILITY*

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Abstract

A new BPM system was used for commissioning and operation of the PIP2 Injector Test Facility. The system of 13 warm and 12 cold BPMs was based upon custom 250 MS/s digitizers controlled and readout over gigabit ethernet by a single multi-core rackmount server running linux. The system provided positions, intensity, and phase for each bpm as a pulse average or pulse waveform from 10 µs to 4.4 ms at a 20 Hz pulse repetition rate.

INTRODUCTION

The PIP-II Injector Test facility was developed to perform an integrated test for the front-end of the PIP-II linac upgrade project at Fermilab [1]. The beamline shown in Fig. 1 includes the warm front-end consisting of the ion source, low energy beam transport (LEBT), radio-frequency quadrupole (RFQ), and the medium energy beam transport (MEBT) sections. It also includes the first two superconducting cryomodules consisting of the half-wave resonator (HWR) module and the 1st single spoke resonator (SSR1) module which are followed a high energy beam transport (HEBT) section with diagnostics and beam dump. The PIP-II Injector provides bunched beam out of the RFQ at 162.5 MHz with pulse lengths from 10 µs to 4 ms at up to a 20 Hz pulse repetition rate with up to 10 mA instantaneous beam current.

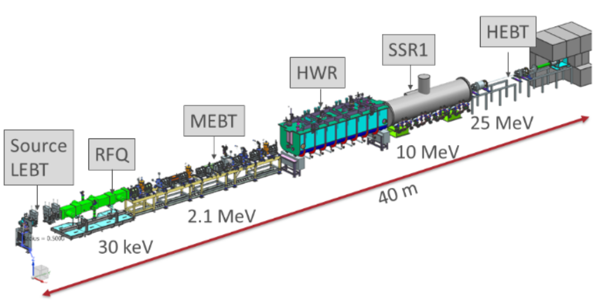

Figure 1: Beamline layout of the PIP-II Injector Test Facility.

After the RFQ, there are 9 warm button BPM pickups in the MEBT section, then 8 cold button BPM pickups in the HWR, 4 cold button BPM pickups in the SSR1, and 4 warm button BPMs in the HEBT. A completely new data acquisition system was developed for the final PIP-II Injector Test run in 2020.

BPM SYSTEM

The new readout electronics are shown in Fig. 2. The main components of the new system are analog signal conditioning modules, custom digitizer modules, a commodity rackmount PC, and Gigabit ethernet control and readback for the system via a standard Gigabit switch.

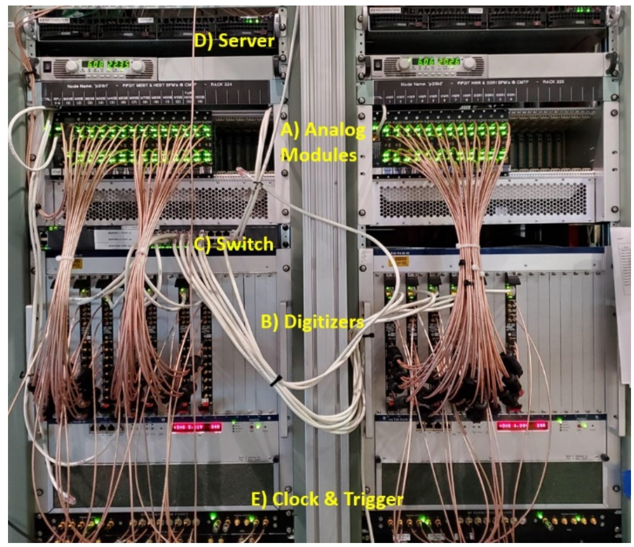

Figure 2: The PIP-II injector test BPM electronics.

Analog Signal Conditioning Module

The Analog Signal Conditioning Modules provide filtering and signal level control (see Fig. 3). There is a 500 MHz low pass filter and programmable 0-32db in 0.5db steps attenuator at the input. A removable daughter card handles the filtering. For PIP-II Injector Test, the daughter card splits the signal to provide band pass filters for both the 1st and 3rd beam harmonics at 162.5 MHz and 487.5 MHz. The daughter card also provides programmable high (26db) and low (6db) gain for each signal path. There is also a variable gain amplifier on the board output with 64 settings from 0-31db. The modules reside in two Eurocard crates which each have a controller board. All settings on each analog module are controlled via ethernet by a raspberry-pi module on the controller board.

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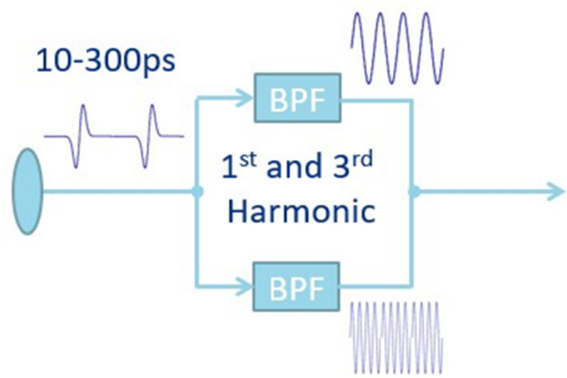

Figure 3: Analog signal conditioning.

Digitizer Modules

A block diagram of the custom digitizer module is shown in Fig. 4. The module was designed in a VME/VXS form factor. It has 8 250MS/s ADCs which interface to the Altera Aria V FPGA via the JESD204B fast serial standard. A dedicated clock chip provides all necessary clocks for the ADCs and FPGA. The clocks are all generated locked to an external 162.5 MHz reference from the low level RF system so that the entire system runs locked to the beam frequency. For PIP-II Injector Test, the module only used the VXS crate for power and cooling. All control and readout occurred over the front-panel Gigabit ethernet connection.

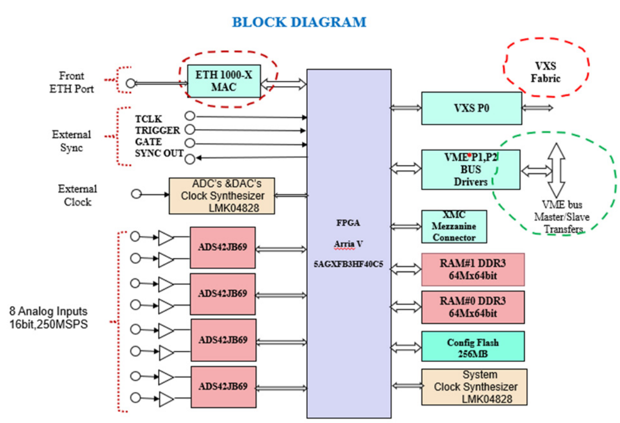

Figure 4: Block diagram for the custom digitizer.

The Digital Signal processing block diagram is shown in Fig. 5 along with the relevant frequencies as a function of the 162.5 MHz RF. The ADC sampling and NCO frequencies for the digital downconverters (DDC) are critical for the phase measurement. Each DDC decimates the signal down to a 1 MHz rate and has 250 kHz bandwidth. Up to 2048 I, Q pairs for each harmonic are stored for each ADC channel on each beam pulse. The data can be further averaged and decimated to record longer beam pulses.

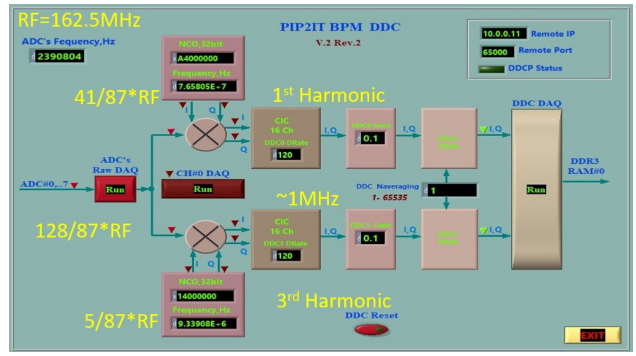

Figure 5: Block diagram for the DDC logic.

Frontend Readout and Controller

The most significant change to the system was moving from a crate CPU board to an external rackmount PC running linux. The rackmount PC interfaces to the digitizer modules via ethernet by way of a standard ethernet switch. The rackmount PC has two 10 Gigabit ethernet interface. One is connected to the switch to talk to the digitizer modules on a private network and the other is connected to the accelerator controls network. The rackmount sever PC has significantly more resources and power compared to the crate CPUs for a fraction of the cost. It is also able to take advantage of a wealth of standard code development tools and routines. The Gigabit ethernet readout achieved 100 MB/s which provides a factor of 10 rate improvement over previous VME implementations. The Gigabit ethernet interface was implemented using Distributed Direct Communication Protocol (DDCP) interface developed at Fermilab. This interface provides methods for talking to hardware including interrupt and streaming features. A block diagram of the interface architecture is shown in Fig. 6.

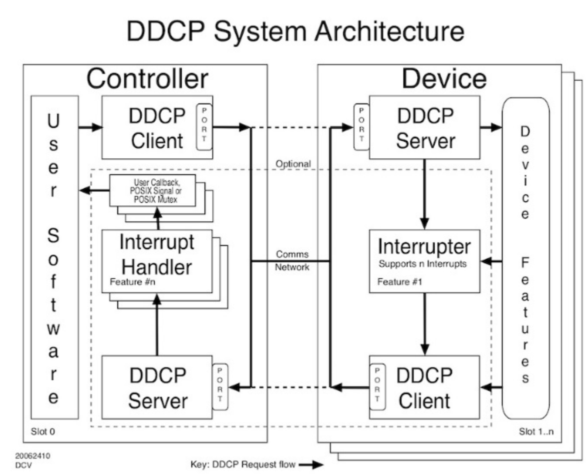

Figure 6: A block diagram of the DDCP architecture.

The frontend controller calculates positions, intensities, and phase from the I, Q data for each BPM. There are four ADC channels for each BPM corresponding to the four pickup electrodes. The digitizers generate I, Q pairs for both the 1st and 3rd beam harmonics for each channel. For PIP-II Injector Test run, 512 samples were readout on each beam pulse for a total of 16 kB per BPM. This allowed the

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data for all 25 BPMs to be easily readout over the Gigabit ethernet bus at 20 Hz.

BPM SYSTEM PERFORMANCE

The BPM system provides measurements of the beam position, intensity for each harmonic, and phase for each BPM. The horizontal and vertical positions are calculated from a 2D polynomial fit [2] to the magnitudes of the 1st harmonic for the four bpm electrodes. For the MEBT, a low β correction is also applied. On each beam pulse, the average as well as the waveform of positions across the beam pulse are available to the accelerator control system. For the nominal commissioning beam pulse of 10 µs and 2 mA, the BPM position resolution was 8 µm. The horizontal position along a 400 µs beam pulse is shown in the MEBT in Fig. 7. The variation at the front of the pulse was determined to be from the RFQ.

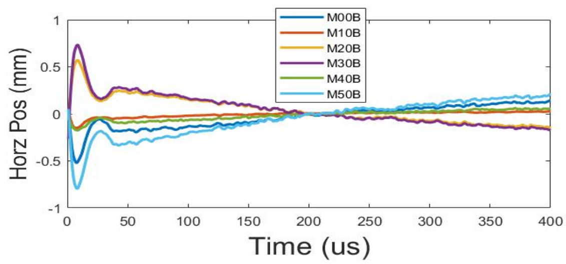

Figure 7: Horizontal positions for a 400 µs beam pulse in the MEBT.

The intensities for both the 1st and 3rd beam harmonic are calculated as the sum of the magnitudes from each BPM electrode. The ratio of the intensity for the two harmonics is related to the bunch length of the beam. Figure 8 shows a plot of the Bunch Factor defined as the ratio of the 3rd harmonic intensity to the 1st harmonic intensity for all 25 BPMs for beam accelerated to 16 MeV after SSR1.

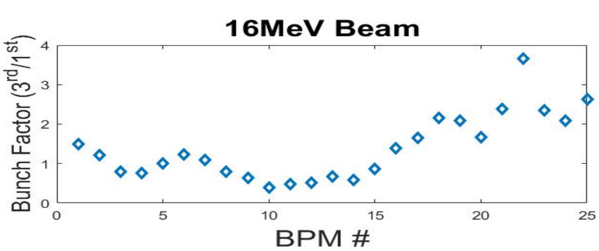

Figure 8: Bunch Factor from BPM intensities along the PIP-II Injector Test beamline for beam accelerated to 16 MeV.

The beam phase with respect to the RF reference is calculated from the 1st harmonic I & Q data. The phase measurement for a 10 µs 2 mA beam pulse was found to have 0.2° RMS. The phase measured for a 4.4 ms beam pulse in the MEBT is shown in Fig. 9. The observed phase oscillation was determined to be caused by the RFQ while the step in the last couple BPMs was caused by the last buncher cavity turning off.

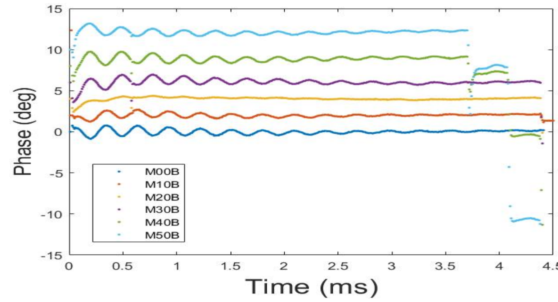

Figure 9: Measured phase along a 4.4 ms beam pulse in the MEBT.

The BPM phase measurement can be used to phase in the RF cavities and to calculate the beam energy as it is a measure of the time of arrival of the beam. To calculate the energy, a technique developed at FRIB was used [3]. This involves calibrating the phase response of each BPM by injecting the same known signal into each BPM cable in the tunnel. Once calibrated, the phase from 3 BPMs can be used to determine the energy. Using this method, the energy in the HEBT was measured with 0.2% resolution which was much better than the measurements obtained from a movable Time of Flight BPM which was over 1%.

SUMMARY

A completely new BPM readout system was installed and commissioned at the PIP-II Injector Test facility. The system imployed a new architecture based upon Gigabit ethernet for readout and control of the digitizer modules using a commodity rackmount server PC. The system was a key diagnostic for the operation of the facility.

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