

NANOSECOND LEVEL UTC TIMING GENERATION AND STAMPING IN CERN'S LHC

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Abstract

The General Machine Timing (GMT) at CERN uses an RS-485 multi-drop network through which messages are broadcast by a Central Timing Generator (CTG) module at a rate of 500 kb/s and decoded by many receiver modules in different form factors. For long distance transmission, optical fibers are used. As a result of cabling and capacitive loading of the receivers' inputs, the timing message signal presents an average jitter of 14 ns at any receiver input. For the LHC era, the 500 kb/s rate will be maintained to ensure compatibility with old receivers. However, a special kind of Phase Locked Loop (PLL), involving digital control in a Field Programmable Gate Array (FPGA) and a DAC to control a Voltage Controlled Crystal Oscillator (VCXO), has been developed to generate a 40 MHz square wave at the receiving side which is locked on average to the timing message signal but presents a jitter of less than 1 ns. This 40 MHz signal is locked to UTC because the encoder in the CTG card uses a 40 MHz clock coming from a GPS receiver, and can be used to generate pulses or to time-tag external events with high precision. The first timing receiver to use this new PLL is the CTRP card in PMC format. This paper describes the CTRP card with a special emphasis on the PLL part.

THE GENERAL MACHINE TIMING

CERN's GMT system guarantees that all accelerators in the complex act as a networked particle production facility [1] by coordinating and synchronizing their activities. The system is based on multi-drop RS-485 networks piloted by CTG cards. On the receiving side, different modules react to messages on the network by arming counters, producing pulses on their front panel connectors or interrupts to synchronize the different front-end computers to events happening in the accelerators. The new generation of receiving modules makes extensive use of FPGA technology and features a special PLL to recover a very stable 40 MHz reference from the 500 kb/s messages. The first module to implement these principles is the CTRP, a PMC card with five output channels. VME, PCI and G64 versions will follow.

CTRP OVERVIEW

Figure 1 depicts the general architecture of the CTRP card. The core logic is implemented in a Spartan IIE family FPGA from Xilinx. This device contains interfaces with the on-board RAM, the HPTDC (High Performance Time to Digital Converter) [2] chip, the PLL and the PLX PCI9030 bridge, therefore allowing memory-mapped PCI access to all these subsystems. The General Purpose Input/Output (GPIO) pins of the PLX chip are used to

reprogram the flash memory containing the FPGA configuration bit stream from the PCI bus. Remote FPGA configuration is a requirement for any receiver card because many of them will be installed in remote places with difficult access, making general interventions a costly operation in terms of both time and manpower.

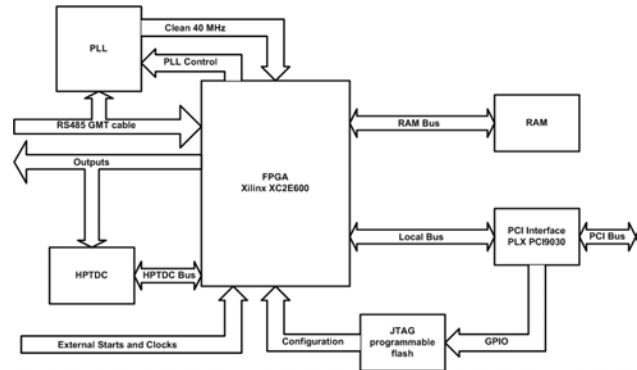


Figure 1: Overview of the CTRP card.

The CTRP receives a UTC time message every second from the CTG. It then starts a 40 MHz count to keep an internal UTC time register with a granularity of 25 ns. This register is used for tagging all the pulses produced by the card.

Software support is provided via device drivers for the Linux and LynxOS operating systems, plus a library implementing an agreed upon interface for clients. This gives us the freedom to change the design and the driver as long as the interface with the client software is not modified.

FPGA Design

The core logic consists of a set of configurable counters. The configuration structure, sent through the PCI bus by the CPU card, contains the following information for each counter:

- The GMT event that will arm the counter.
- The start mode. A counter can be started immediately after the arrival of its associated event or wait for a start pulse in any of the cards start inputs. It can also be started by the output of the previous counter.
- The clock mode, which specifies the clock to be used by a counter. Besides any of the external clocks coming to the card via its front panel, the counters can count ticks of the 40 MHz produced by the PLL. Because this 40 MHz is synthesised from the GMT message, it is locked to UTC, therefore enabling the module to produce UTC-related pulses with a precision of 1 ns and a resolution of 25 ns.
- A field specifying whether the output of the counter will be routed to a front panel connector, to the PCI

bus as an interrupt or both. This feature is very useful to synchronise real-time tasks running in the CPU card.

The FPGA is also responsible for decoding the incoming messages and the subsequent RAM lookup scanning for actions to take after reception of a given message. Besides this, it also hosts the phase detector and the digital controller for the PLL.

The PLL

The current generation of timing receiver modules uses the DP8343 receiver/decoder chip from National Semiconductor to receive and decode the GMT messages. Conversely, the DP8342 companion chip is used to encode and send the GMT messages. The DP8343 samples the incoming message with a free-running on-board 16.384 MHz quartz oscillator. Each receiver therefore validates incoming messages with an inherent jitter of one period of this clock.

For the new generation of cards, we respect the format of the messages and the 500 kb/s rate to ensure backwards compatibility with existing receivers, but an analogue-digital hybrid PLL has been designed to recover a 40 MHz clock from the message. The goal is to recreate in every receiver the original 40 MHz clock used to encode the messages, with a precision better than 1 ns, cleaning in the process the cable-induced 14 ns of jitter present in the bit stream. In order to achieve this precision with a frequency multiplication factor of 40, the special architecture of figure 2 was chosen.

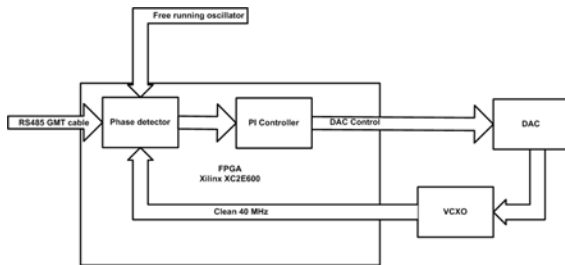


Figure 2: PLL architecture.

The phase detector is a simple counter counting ticks of an unrelated free running oscillator between the rising edges of the incoming message and the clean 40 MHz. Averaging a suitable number of measurements does the statistic cleaning needed to overcome the inherent limitation of 1 tick in the precision of the measurements. Too big an average would however penalize performance by making the whole loop slower. The phase detector is followed by a PI controller with programmable proportional and integral coefficients, the result of which is fed to a DAC for VCXO control. The programmable coefficients provide a very versatile solution that can be applied in many situations [3].

The HPTDC chip

As mentioned above, the FPGA can time-tag every pulse produced by the CTRP with a granularity of 25 ns.

To get finer resolution, an HPTDC chip was added to the card. This chip provides a free-running time tag of all the pulses we feed to it. Since the HPTDC does not know anything about UTC, we also time-tag a reference 10 kHz pulse train produced by the FPGA in synchronism with UTC. By comparing the free-running time tag of a given 10 kHz tick to that of our pulse of interest, we can work out the exact UTC time for the pulse to within 1 ns.

The HPTDC was developed at CERN to satisfy the requirements of the Time of Flight subsystem of the Alice detector. It is capable of time-tagging pulses with a precision of 25 ps in high resolution mode.

As figure 3 shows, the coarse tagging of the HPTDC is based on a clock signal fed from the board. The nominal frequency for this signal is 40 MHz which is fortunate because that is exactly the frequency of our cleaned clock. The chip then multiplies this frequency by a factor ranging between 1 and 8 using an analogue PLL. The choice of this factor is dictated by the resolution mode we request. Higher resolution implies higher frequencies and therefore higher power consumption. The output of the PLL is then fed to a Delay Locked Loop (DLL), a chain of 32 controllable-delay taps with feedback that will ensure the alignment of rising edges at its input and output. After equilibrium is reached, we find the input signal delayed by $T/32$ after each tap, T being the period of the input signal. By freezing the state of all the taps and that of the 40 MHz counter at the arrival of a given pulse, we obtain a time tag whose precision is exactly one tap. In our case, the resolution of 25/32 ns obtained in the least precise mode is more than enough.

The initial configuration of the HPTDC is done through an on-chip JTAG port connected to the FPGA. The FPGA maps each JTAG line to a bit in a register that can be accessed by the CPU in read and write mode. Therefore, the burden of handling the JTAG protocol is passed on to the software. Time tags are stored in a FIFO and read out via a parallel port.

FUTURE DEVELOPMENTS

The CTRP is the first in a series of receiver modules to be developed. In the immediate future, VME and PCI versions will follow. The PCI card will be used to drive the external Cycle Start input of the WorldFIP master cards for the control of the power converters in the LHC. The VME version will become an essential ingredient in any new VME installation, replacing the TG8 module [4]. On the other hand, a G64 version of the card will allow us to replace the oldest receivers in the accelerator complex, the TG3s [5], which currently impose constraints on the timing system due to their limited bandwidth and their non-programmable nature. All of these cards will be seen by the users though the same software interface. With manpower shrinking and new accelerators coming, reducing diversity for the future is a key goal.

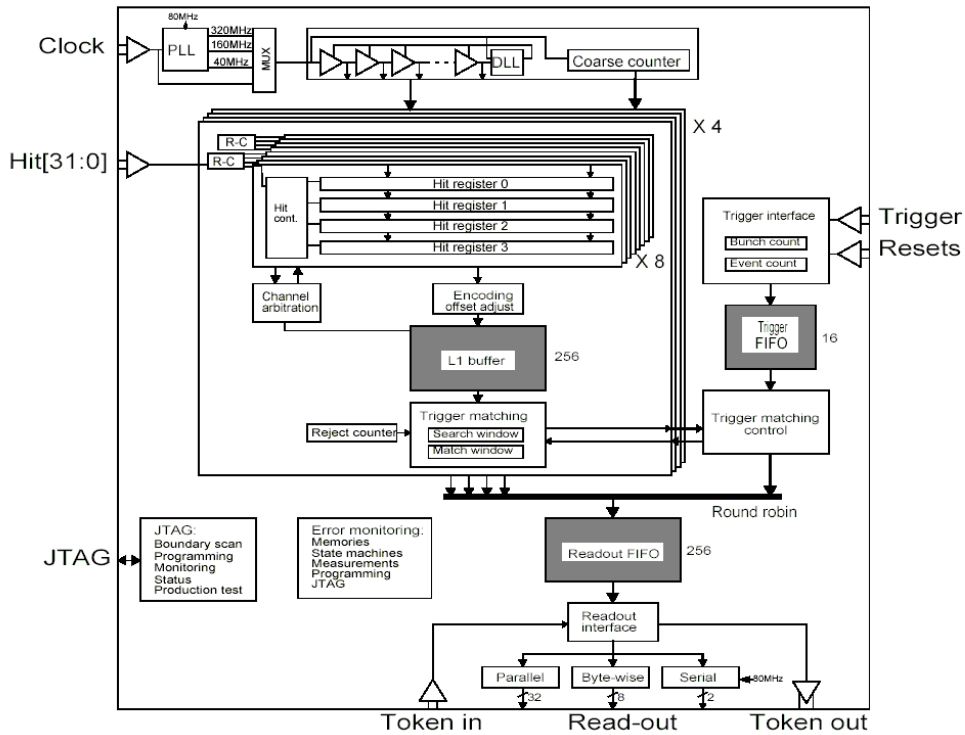


Figure 3: HPTDC internal architecture.

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