

# THE EVOLUTION OF THE CERN SPS TIMING SYSTEM FOR THE LHC ERA

Julian Lewis, Jean-Claude Bau, Javier Serrano, David Dominguez, Pablo Alvarez Sanchez CERN, Geneva, Switzerland

## Abstract

The SPS is the last machine in the LHC injector chain; however, it will be difficult in the LHC era to treat it like the other lower energy multi-cycling machines. Not only is there a huge amount of legacy hardware and software, but due to machine physics constraints, it is doubtful that it would ever be possible for the SPS to truly multi-cycle in the PS sense. Today, the SPS control system regularly performs super-cycle changes in an average time of 20 minutes, but then setting the beams up afterwards takes longer. We expect many more SPS super-cycle changes per day in various LHC filling scenarios, and machine developments, and hence any savings we can make in SPS super-cycle switch-over time will not only better exploit the PS complex, but will also provide more SPS beam for other users. Centrally coordinated sequence changes make obvious gains for physics, but also, the cost benefits of a uniform approach to controls have been identified elsewhere. This paper will discuss the planned central-timing due to come online in November 2003.

## INTRODUCTION

To fill the LHC requires chains of accelerators, each performing operations on the beam before passing it on to the next stage. These chains are dynamically set-up to produce both ion  $Pb^{82+}$  and proton particle beams. For protons, a low intensity  $5 \times 10^9$  pilot beam is needed to test the LHC settings prior to injecting of the nominal bunch intensity  $\sim 1.1 \times 10^{11}$  at 450 GeV. The injector-chains in the ion and proton beams involve different accelerators. For protons, the chain consists of a 90 KeV source and RFQ, a 50 MeV proton Linac (Linac-I), the 1.4 GeV Proton Synchrotron Booster (PSB) with 4 rings, the 26 GeV Proton Synchrotron (PS), and finally the 450 GeV Super Proton Synchrotron (SPS). For ions an Ion Linac (Linac-II) injects directly into the Low Energy Ion Ring (LEIR), then on to the PS and SPS. The LHC has two rings which will be filled simultaneously batch by batch from the SPS. Any faults during the filling process will require dumping the beam in the injector chain and then trying again for the same batch in the LHC ring. In addition to this, the SPS accelerator must still serve other physics users such as Fixed Target and CNGS, and also machine development cycles. These new SPS requirements imply that many more SPS cycle sequence changes will be needed than at present, and hence a more dynamic cycle sequence control is needed.

## SPS CENTRAL TIMING FOR LHC

With the exception of the SPS, the Central Beam and Cycle Manager [1] (CBCM) has been sequencing

CERN's accelerators for several years. These lower energy machines permit, to a limited degree, treating machine cycles independently of their position in the cycle sequence, and hence ignoring effects such as remanent magnetic fields. This is possible because in the PS machine the B-field is forced nearly to zero ( $< 50$  Gauss) between each cycle. Also, because the B-field goes to zero, each accelerator cycle can be composed of an integer number of basic time periods corresponding to the Linac repetition rate, which is the fastest cycling machine in the injector chain. The basic period clock set by the Linac repetition rate provides the pulse of the central timing, and all other timings are derived from this pulse. However, the SPS main power requirements and the implied loss of machine beam time would not permit treating SPS cycles in this way. Hence if the CBCM is to pilot the SPS timing, each SPS cycle instance must be treated uniquely; each SPS cycle will not in general contain an integer number of basic time periods. The start and end times are strongly determined by the B-field of the neighbouring cycles in the sequence. The CBCM currently provides very flexible real time cycle sequence control of the SPS injectors and other accelerators in the PS complex, and, bearing in mind the new SPS requirements, a project has been undertaken for the inclusion of the SPS into this scheme by November 2003. This has forced us to find some new concepts so that the apparent CBCM and SPS incompatibilities can be accommodated, and a new central timing system built to handle them. At the same time we have taken the opportunity to revise all of our basic timing hardware.

## THE HARDWARE

The timing provided by the CBCM is carried by dedicated networks. Two types of networks will be present, the General Machine Timing (GMT) [3] which is RS485 based, and the Beam Synchronous Timing (BST) [2], based on the CERN Timing Trigger & Control (TTC) [5] standard. A single hardware card, named the "CTG", with two different FPGA configurations, drives both network types.

### *The General Machine Timing networks*

Seven CTG cards, with the GMT configuration, will drive seven GMT timing networks, each network providing up to eight 32-bit events per millisecond with better than 1ns precision. The event encoding clock is 40.000 MHz and provides a Manchester encoded serial bit stream at a rate of 500K bits  $s^{-1}$ , phase locked with the GPS "One Pulse per Second" (1PPS) [4]. Each network is associated with a particular group of accelerators, such

as LEIR and Linac-II for ions. The GMT networks carry machine events, the 1 KHz coarse timing clock, Telegrams [1], which describe the current beam parameters, and the UTC time.

### The Beam Synchronous Timing networks

There will be an additional four BST versions of the CTG to drive the LHC and SPS beam synchronous timing with 25ps precision. The BST cards are supplied with the RF bunch clock  $\sim 40.0789$  MHz and revolution clocks, 23us for SPS and 89us for LHC. The BST message is a byte stream sent each revolution, and is Manchester encoded using the bunch clock. The BST messages carry triggers for beam instrumentation equipment, the UTC time, and parameters from the Telegram. The extremely high precision is possible because the physical transport layer uses the TTC hardware.

### Reference clock generation

The CBCM contains its own clock generation which once initialised can run independently of the Global Positioning System (GPS). The One Pulse per Second (1PPS) signal is initially obtained from a commercial GPS satellite receiver, and a synthetic version is manufactured from a 10 MHz voltage controlled oscillator. By adjusting the period and phase of this clock, the system phase locks a synthetic 1PPS with the GPS version to within 20ns, the locking process may take hours to complete. The final 10 MHz local clock has a drift of less than one part in  $10^{-11}$  per Month. These two signals, the local 10 MHz clock, and the synthetic 1PPS, are fed into the CTSYNC [4] reference clock generator in the CBCM. The CTSYNC produces the 40.000 MHz event encoding clock for the GMT, the basic period or Linac repetition rate clock, currently 1.2S, the 1 KHz coarse timing clock, and a 1PPS clock advanced in time by 100us for later cable length delay compensation. All these reference clocks are in phase with the advanced 1PPS, so that ticks of the 40.000 MHz correspond to 25ns increments in the advanced UTC second. Once the system is running, all that remains is to set the Second number of the next 1PPS, and the system is then locked to UTC. The required precision for setting the CBCM clock in this way is  $\sim 400$  ms, so even the Network Time Protocol (NTP) could be used.

### Timing reception

Currently new timing receiver modules for both the BST [8] and the GMT networks are being developed. The new GMT timing receiver, the CTRP [3], will come in PMC, PCI, VME and G64 formats with both LynxOS and Linux drivers. There are also many legacy hardware modules such as the TG8 [6] which impose the 500K bit rate, and the RS485 standard, and hence backwards compatibility on the CTRP and CTG-GMT. None the less we are still able to obtain very low peak to peak jitter ( $< 1$ ns) by including an on board 40.000 MHz PLL [4] based on a Temperature compensated voltage controlled crystal oscillator (TCVCXO) which is digitally controlled

through a DAC, the PLL logic is implemented in the main FPGA of the receiver card. Thus the CTRP is able to regenerate the original 40.000 MHz encoding clock, and is further able to UTC time stamp each 25ns clock tick. The CTRP also incorporates the CERN High Precision Time to Digital Converter (HPTDC) [7] chip. This chip driven from the 40.000 MHz will allow us to UTC time stamp CTRP signals to within 1ns. The CTRP has either 5 or 8 fully configurable 50MHz 32-bit counters, and hence it is able to provide pulse bursts and divided clocks at its outputs. Two external start and two external clock inputs are available, so that counters can use the bunch clocks and revolution frequencies to provide beam synchronous timing pulses. The 40.000 MHz clock is also used to drive a digital event delay, and hence compensate for cable delays to within 25ns by making up the 100us of the advanced 1PPS. The precise compensation values used can be obtained by various means depending on the needed precision; by dead reckoning, from measurements base on reflectometers, and finally, by referencing the beam itself.

## NEW CONCEPTS

The CBCM logic must accommodate the SPS variable cycle lengths, and also be able to match the PS injection energy (14 GeV or 26 GeV) which in turn determines the base line B-field of the SPS cycle sequence [Fig 1]. To switch from a 14 GeV cycle sequence to one at 26 GeV would obviously need ramping functions in the power converters. Thus a cycle sequence must be preceded by a lead in function, and appended with a lead out function so that the different base energies can be matched. In [1] the basic concepts of *Cycle* and *Compound-Cycle* are explained. The accelerators controlled by the CBCM sequence logic form a network; the machines are the nodes and beam transfer lines are the arcs. The beams produced in this network require executing cycles on one machine after another until the final beam characteristics are achieved. This set of cycles is the Compound-Cycle or "Beam" for short. By this definition, a Beam is a data structure that contains data needed by the CBCM, such as the cycle durations and their relative phases, needed to schedule in advance the activities of the accelerators under its control. Ordered collections of Beams can be arranged to specify the operational requirements for the entire network. They might have names like

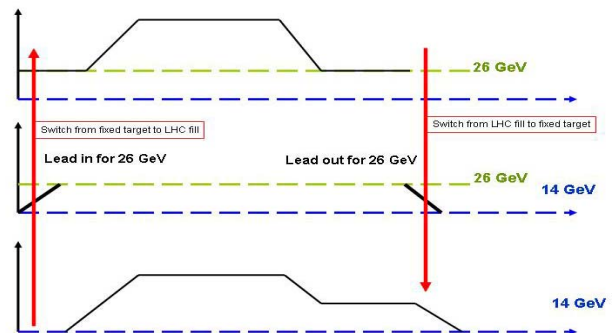


Figure 1 : Cycle sequence changes 14 to 26 GeV

“LHC-Filling” or “Fixed-Target + MD”, and each collection may contain many compound cycles, i.e. Beams. Such a collection of Beams arranged to perform a task like LHC filling is a Beam Coordination Diagram (BCD), and occupies one “level” on the CBCM; there are a total of 32 levels available. Hence switching between the level containing the BCD for LHC-Filling and that containing Fixed-Target + MD moves the whole CERN accelerator complex from one task to another, and hence fulfils the main requirement, namely a rapid automated sequence switch. However, the LHC-Filling sequence requires injection from the PS at 26 GeV, while the Fixed-Target + MD sequence has a 14 GeV base energy, so a ramp is required to switch between these sequences. We must extend the concept of BCD to that of “Sequence”, and define Sequence as: A set of BCDs and their termination conditions for one network task [Fig 2]. The termination condition may be a repeat count, typically “1” for lead-in and lead-out BCDs, and a Boolean expression for the main BCD, which repeats until it becomes false. Thus the CBCM is now switching between Sequences, each Sequence being comprised of a set of BCDs and their termination conditions. Typically then, a Sequence will contain 3 BCDs, and each BCD pilots not only the SPS, but all of its injectors. The SPS is “Strongly Coupled” [1] in time with its injectors.

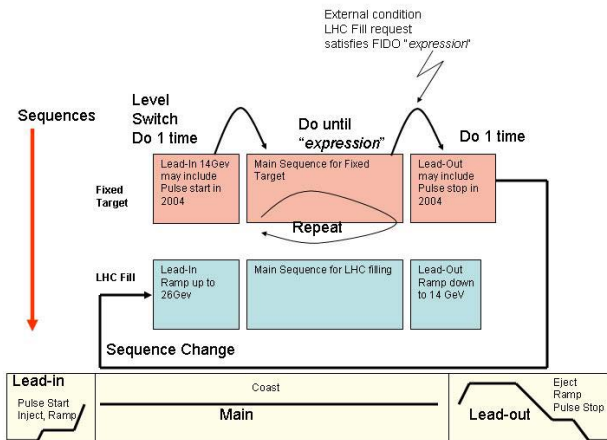


Figure 2 : Sequences

## CONCLUSION AND FUTURE

The tests of this system are scheduled for November 2003, so until now none of the components described herein has been tested on the real accelerator network. However, BCD changes are common in the PS complex, and we believe the extensions mentioned are enough to cover the SPS requirements. In 2004, two major additions will be included, first for the LEIR and Linac-II to provide the LHC with Ions, and towards the end of 2004 we will add the LHC itself. This will undoubtedly provide enough material for another ICALEPCS paper, wherever that may be.

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