IMPLEMENTATION AND INTEGRATION OF THE SNS TIMING AND MACHINE PROTECTION SYSTEMS

Coles Sibley, Alan Jones, Dave Thompson (SNS-ORNL) Eric Bjorklund (LANL)

Abstract

The Spallation Neutron Source (SNS) under construction in Oak Ridge, TN will produce high intensity neutron pulses using a linear accelerator and an accumulator ring to put $1.5x10^{14}$ protons/pulse onto a liquid mercury target at 60 Hz. The timing and synchronization system for this facility consists of two globally distributed links, an 'event link (EL)' for triggers and a 'real-time data link (RTDL)' for data. This system was originally designed for RHIC, and was modified for SNS requirements. A 'Machine Protection System (MPS)' protects the accelerator against equipment failure and excessive beam losses, dependent upon the operational mode of the accelerator and the beam dump in use. These two systems are tightly integrated. The operational mode is distributed on the RTDL. The MPS uses the timing system to assure operation within specified duty cycle and pulse width limits. In addition, information on shut-down causes originating with the MPS is broadcast by the timing system for post mortem analysis. The status of implementation of these two systems, and experience during the commissioning of the front end will be presented. Some tools for post mortem analysis and plans for the future will be discussed.

MPS - TIMING SYSTEM OVERVIEW

The SNS timing system is based on the RHIC timing system at Brookhaven National Lab[1]. The timing master IOC defines the machine super cycle based on requests for various system rates, power limitations and system coincidence requirements for beam production. It uses a number of timing input modules to trigger event outputs and broadcast system parameters.

The global outputs are the EL that broadcasts events on a carrier phase locked to the ring revolution frequency and the RTDL that broadcasts machine data. The events can be generated in hardware or software. The RTDL data includes beam dump and pulse width / power limitations that are used by MPS. The following RTDL frames are used by the Machine Protection System (MPS):

1. Time of Day (TOD) - Used for high precision time stamps for post mortem analysis and MPS heartbeats.
2. MPS Mode - Defines machine and beam mode parameters for mode masking MPS inputs.
3. CRC Frame - Used to validate all frames broadcast during a machine cycle.

The MPS uses the EL clock to generate two interlock carrier signals, the Fast Protect Latched (FPL) and the Fast Protect Auto Reset (FPAR). The decoded events are used to trigger resets, create 60 Hz interrupts for heartbeats, and trigger logic for the RTDL transmit and RTDL valid events. The MPS chassis are distributed around the facility for system inputs to shut off the beam if a system faults that will cause beam loss. FPL inputs are used when a system reset is required and FPAR is used when the fault can clear before the next pulse.

Two timing system boards designed at BNL provide IOC's with an interface to the timing system, the V124S timing trigger generator and the V108S utility module. The V124S provides gates or triggers based on events from the EL with programmable delays, widths, and trigger events. The V108S provides software interrupts based on events and decodes the RTDL frames from the RTDL carrier. It also provides system monitoring capabilities and remote reboot capability. This is the module that provides system-wide IOC time for synchronous data acquisition. There is also an MPS output used for software monitoring of signals that need to provide an MPS input independent of the network.

MPS - TIMING INTERFACE

There are three subsystems making up the MPS: the MPS master and interlock hardware, an MPS PLC, and a trigger control chassis. The timing system connects to the MPS master and the trigger control chassis through the EL and RTDL. The MPS sends fault triggers to the timing master from the trigger control chassis to produce MPS fault events. High-resolution time stamps are used for post mortem analysis. These are created from the TOD frame on the RTDL and fast fault timers on the inputs using the EL clock.

Beam and Machine Mode Setup

MPS PLC inputs include the beam mode and machine mode from a hardware key switch. A key switch is used so the machine can be "locked" in a power mode for operational control. The MPS PLC reads key switch position:

Table 1. Beam Mode and Machine Mode definitions.

Beam Modes	Off	Standby	MPS Test	10 usec
	50 usec	100 usec	1 msec	Full Power
Machine Modes	Source	D_Plate	CCL Beam Stop	Linac Dump
	Injection Dump	Ring	Extraction Dump	Target

The IOC scans the PLC tags into EPICS. The timing master IOC reads these process variables (PV's) and broadcasts the machine mode and beam mode on the RTDL. The MPS master IOC reads the modes from the RTDL and writes the result to the PLC. During the

handshake, the timing master puts the system in standby mode through the Trigger Control Chassis (TCC). When the MPS master writes these to the PLC, the handshake is complete. There is a timeout that puts the system in a fault condition and shuts down the system if the two do not agree in 250 msec.

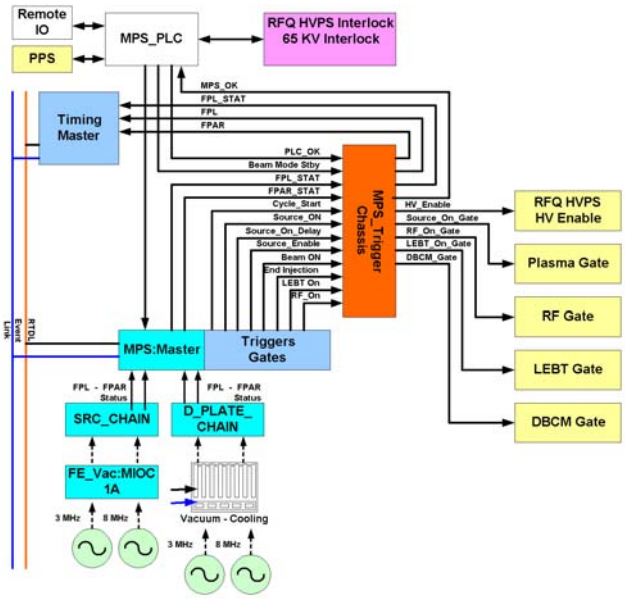

Figure 1: Machine protection system and Timing system interface.

MPS uses the beam and machine mode to mask inputs not required for the present mode of operation and allows systems to operate as the beam mode permits. For instance, insertable devices can withstand 50 usec of 38 ma beam and are masked during short pulse operation. A 100-usec beam pulse can destroy the device which is therefore not masked for 100 usec or longer beam. If the device leaves the home position the beam is shut off. Due to the sensitive nature of masking inputs, this has to be very robust. The RTDL sends 24 bits of data per frame and uses a CRC check for each frame. The modes are encoded three ways in the RTDL frame to detect single or multiple bit errors. In addition, a 24-bit CRC check is added in frame number 255 [2]. This virtually guarantees reliable data, or detection of an error. The machine will not provide beam if there is an error in the mode mask. The mode masks are set up in an Oracle application and are tightly configuration controlled. They are down loaded to hardware during an IOC reboot and integrity checked pulse to pulse.

The timing master uses the beam mode and EPICS record processing to set the start and stop times of events, and to enable RF, beam, and related events. Synchronization of events for beam on and RF on is described in SNS tech notes 99 and 100[3,4]. A chopper in the low-energy beam transport (LEBT) line will be used to limit beam power as a function of beam mode. The system is not yet in place, and power is now limited by limiting the pulse width by limiting RF gate coincidence time[5].

Trigger Control Chassis, Controlling Beam generating hardware

The MPS master uses a V124S to trigger inputs to the TCC. The TCC provides gates to critical devices such as the RFQ, LEBT chopper, and source RF or PLASMA. The lack of any one of these gates will cause the beam to turn off [6]. During a machine mode transition or in the case of a fault (PLC inputs and echoes do not agree) the PLC sends a shift or a fault to the trigger control. A fault causes RF plasma gate to turn off while a standby causes the gates to be non-coincident. When the TCC receives a standby or fault signal, any coincidence between the plasma gate and the RFQ gate outputs will latch a fault to the PLC causing the ion source 65 KV supply and the RFQ high voltage to turn off for a fail safe fault condition.

In addition a gate is provided to the Differential Beam Current Monitors (DBCM) to integrate beam loss between two current transformers. Figure 1 shows how the Trigger control chassis centralizes the pulsed inputs with the asynchronous events. Figure 2 shows the distribution of input triggers and output gates for several scenarios.

An FPAR fault will turn off the RFQ and plasma gates for the duration of a cycle. If the fault persists at the next cycle start event, the Source-On pulse is inhibited and the Source-On-Delay is propagated for thermal stability reasons. An FPL fault will turn off the RFQ gate and the Source-On gate. The gates will not be retransmitted until the fault is cleared. This condition leads to thermal instabilities of the RFQ resonance cooling system and takes ~5 minutes to recover. We are looking at alternatives to turning off the RFQ on a latched fault, such as a high-speed switch and crowbar on the 65 KV power supply in the ion source.

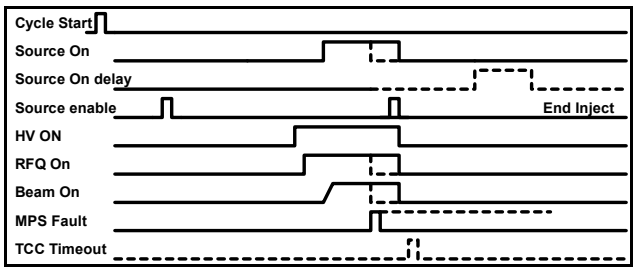

Figure 2: Timing system gates and MPS inputs.

POST MORTEM

Event Triggers

When an MPS input faults, the MPS master sends an input to timing master's V124. This generates an MPS fault event. There are two types of faults, FPL and FPAR. The FPL causes one event to go out with minimal delay for use in transient recorders, scopes, etc. The FPAR also causes one event to be broadcast with minimal delay and a second event that is delayed for ~8 msec to allow data acquisition boards to transfer all data to the CPU using channel access. These events are throttled to a 6 Hz rate, as they can fault at 60 Hz.

Figure 3 illustrates triggering a scope on an MPS event. In this case we were faulting the MPS system for response time studies. Several applications are being written to capture numerous waveforms triggered off the MPS events. PV's triggered from these events instead of getting continuously processed will greatly reduce the network traffic required for post mortem analysis. This helps for beam-related waveforms and RF waveforms that are usually triggered at a faster rate than the beam, at least during commissioning.

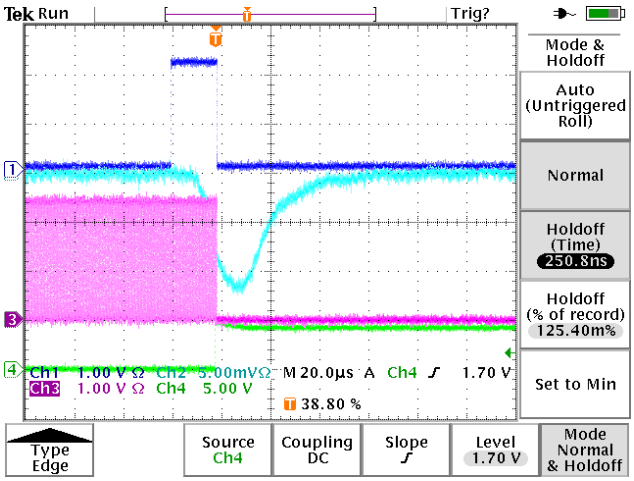

Figure 3. MPS Test fault to measure fault response in system. (1) Beam on gate. (2) Electron dump current in the source. (3) FPAR carrier signal. (4) Output status of the FPAR chain going to the timing master to generate an event.

First Fault Detection

The MPS system uses the EL clock as a high speed timer for fault detection. This runs at ~16.9 MHz and counts from the cycle start event to a fault in a local MPS chassis. This high-speed count is converted to nanoseconds and is added to the cycle start event time from the RTDL. Faults are "caught" by the MPS Post mortem program that uses the time stamp correlator and displays the faults within a cycle in the order faulted. Figure 4 shows two RF faults and the carrier fault event in the MPS master.

REMAINING ISSUES

During the initial commissioning period noise was causing numerous trips and CRC / parity errors in the timing system. This was resolved after an unintentional ground loop was discovered. MPS is still plagued with false trips induced by noise generated from the high voltage converter modulators and from sparks originating in the source. These are being filtered and drive signal levels increased to reduce the trips. Efforts are under way to reduce the noise at the source.

Beam power limits are straight forward to implement but the lack of the LEBT chopper presents some difficulties. An integrating current monitor in the MEBT will provide a hardware limit for the produced beam.

One major problem with the initial implementation is a lack of time stamp synchronization between the VME-based IOC's and the PC-based Network Attached Devices (NAD's) introduced by the diagnostics group for beam instrumentation. Although this is not directly a problem in the timing system it needs to be resolved. Time synchronization is presently relying on NTP and does not always provide the resolution needed for 6 Hz operation. A PCI card has been designed by the diagnostics group to alleviate this problem. This should be in production before the end of the year.

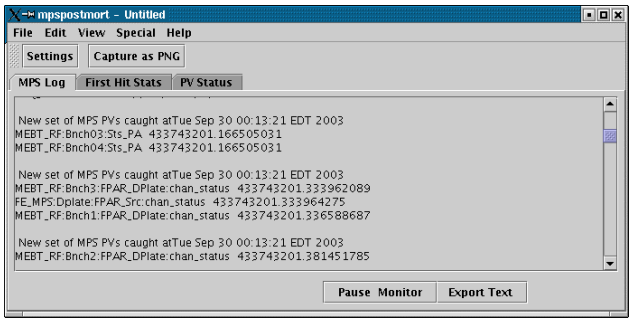

Figure 4: First Fault indication

CONCLUSION

The MPS and Timing systems has proven to very reliable. During the past year there have been very few reboots during operational periods. The timing system and the MPS are strongly interdependent and have worked well together. There have been no faults due to mode masking MPS inputs from the timing system at 60 Hz. The MPS has been shown to cut off the gates within the required 20 usec. The LEBT chopper will improve the beam extinguishing time to the 5 usec level for front end faults as required.

REFERENCES

[1] B. Oerter, "SNS Timing System Requirements Document" Internal Documentation (SNS 109020000-SR0001 Rev1)

[2] E. Bjorklund, "Cyclic Redundancy Check Codes Used in the SNS Real-Time Data Link", SNS ASD Tech note #45

[3] E. Bjorklund, "A Metric for Measuring the Evenness of Timing System Rep-Rate Patterns", SNS ASD Tech note #100

[4] E. Bjorklund, "The Theory of Rep-Rate Pattern Generation in the SNS Timing System" SNS ASD Tech note #99

[5] C. Sibley , "SNS Run Permit System", Paper TUAP023, 2001 Particle Accelerator Conference

[6] G. Dodson, "Beam Extinction Measurements in the SNS Front End Systems", SNS ASD Tech note #100