RECONFIGURABLE TIMING CONTROLLER USING PLDS

N. Hosoda, T. Ohshima, K. Kobayashi, T. Aoki, H. Ego, K. Fukami, Y. Kawashima, Y. Ohashi, T. Takashima, H. Yonehara, SPring-8, Hyogo 679-5198, Japan

Abstract

We developed the reconfigurable timing controller (RTC) using programmable logic devices (PLDs) for the SPring-8 timing system. The RTC uses three complex PLDs (CPLDs). The RTC equips 20 LEMO connectors for the signal I/O and 80-pin flat cable connectors for remote control. We prepared a CPLD configuration circuit with a D-sub connector in the RTC for in-system programming. Therefore, we can program the logic data in CPLDs of the RTC without removing the RTC from NIM crate. We replaced many NIM modules for logic circuit of the timing system by the RTC. This replacement downsized the timing system and reduced maintenance cost. The adjustment of the system became easy. New functions for top-up injection were prepared in the RTC. Test operation of the top-up injection has begun in September 2003. The RTC is well working. The RTC has the flexibility and expandability. If new functions are requested to the timing system, then we can add these functions without increasing the modules.

INTRODUCTION

The SPring-8 timing system provides trigger signals for accelerator machine and apparatus of synchrotron radiation experiments. Many trigger signals concerning injection sequence are made at one place. Each trigger signal is distributed to machine components using optic fiber link [1]. Time delays, time widths and signal levels are different in trigger signals. To make these signals, we have used many numbers and kinds of NIM modules such as logic units, gate/delay generators and cable delays. In addition, many cables were used to connect NIM modules. A lot of modules, cables, and connectors caused the timing system failure, though it was rare. When the failure occurred, it was hard to trace the signal. Moreover, because arrangement changing of modules and adjustment of settings were necessary, it was difficult to add new functions. Since top-up injection is planned to begin in autumn 2003, we must add new functions to enable it to our timing system. We want to reduce the number of NIM modules and to add new functions.

WHY PLD ?

First, we checked our timing system. We adopted off-the-shelf NIM modules. The functions and the number of channels of some modules are insufficient for our demand. This increases the number of NIM modules.

Our timing system works by a common clock generated from 508 MHz RF and 60 Hz AC line. We can control electron bunch filling of the storage ring by using the common clock. Trigger signals, for example linac electron gun trigger, must synchronise to the common clock. These trigger signals were generated at the asynchronous circuit as shown in Figure 1 (a). This circuit use logic modules, pulse-extend module and delay modules. According to timing condition of input signal A, signal C does not synchronize with input signal B as shown in Figure 2 (a). Therefore, we always excluded first pulse of signal C. This method by the asynchronous circuit also increases the number of NIM modules. The pulse width and the delay in the asynchronous circuit were rigidly defined. The adjustment of these values was hard.

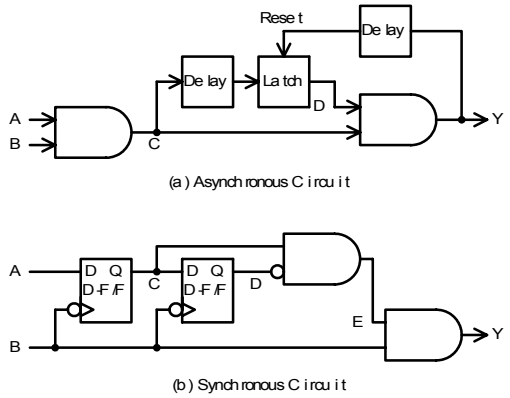

Figure 1: Block diagram of (a) asynchronous circuit and (b) synchronous circuit.

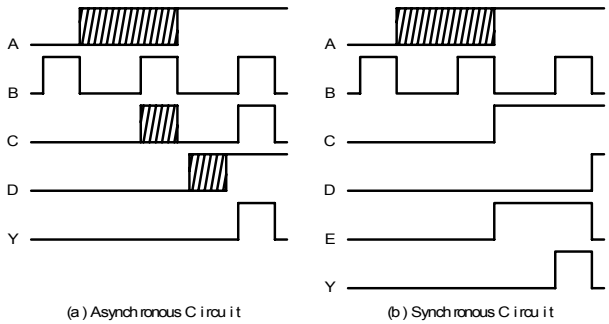

Figure 2: Timing chart of (a) asynchronous circuit and (b) synchronous circuit.

Recently programmable logic device (PLD), such as complex PLD (CPLD) and field programmable gate array (FPGA), is used in much kind of machines. We found out that the PLD is suitable for our timing system by following reasons.

Our timing system works by a common clock. All logic units in the synchronous circuit also work by a common clock. Our timing system can reconstruct by the synchronous circuit. The reconstruction of the asynchronous circuit into the synchronous circuit is

simple. Figure 1 (b) shows synchronous circuit only using logic components. As shown in the timing chart of Figure 2 (a) and (b), output signals Y of the each circuit are same. PLD is suitable for the synchronous circuit. If we reconstruct our timing system by the synchronous circuit, then we can program almost functions of our timing system into the PLD. It downsizes the timing system. In addition, we can program the logic circuit in the PLD repeatedly. The modification of the circuit becomes easy.

We decided to substitute PLDs for many NIM modules of our timing system.

HARDWARE

RTC

We developed the reconfigurable timing controller (RTC) using CPLD. The RTC is a twice width NIM module. Figure 3 shows the block diagram of the RTC and I/O interfaces to the other devices.

We can make the circuit of the RTC simple by using CPLD. Because CPLD have electronically erasable programmable read only memory (EEPROM) cells and work without any external ROM. We adopted three XC95108PC84 CPLDs manufactured by Xilinx. This CPLD has 108 macro-cells and 84-pin plastic lead chip carrier (PLCC). The number of macro-cell is small, but wiring of this package is easy. This is the reason we select this CPLD.

The RTC has a lot of signal I/O. Total 20 LEMO connectors are prepared. We can control remotely the RTC using a VME TTL DIO board. The RTC receives counter values as 24-bit serial code through three signal lines (data, clock and strobe) from VME TTL DIO board.

A 508 MHz synchronous universal counter (SUC) generates a frequency-divided clock and a delayed frequency-divided clock synchronising with the 508 MHz RF signal [2]. The RTC can set the delay count to a SUC. We prepared a CPLD configuration circuit with a D-sub connector in the RTC for in-system programming. Therefore, we can program the logic data in CPLDs of the RTC without removing the RTC from NIM crate. Table 1 lists the I/O interfaces of the RTC.

A 16-character × 2-line dot matrix liquid crystal display (LCD) on the front panel of the RTC displays counter values. A toggle switch is prepared on the front panel of the RTC to reset the counter values.

To ramp up the energy of the electron beam from 1 GeV to 8 GeV at the booster, 10 kHz Fast DO boards of VME control magnetic field strength of main magnets and an RF acceleration voltage. An important condition to ramp up is to change all magnetic field strength and the acceleration voltage synchronously by using a clock generated from single source. We use a 10 kHz crystal oscillator to generate a ramping clock for these fast DO boards.

Table 1: I/O interfaces of RTC

I/O	Logic Level	Connector	Number
I	NIM	LEMO	2
I	TTL	LEMO	2
O	TTL	LEMO	16
I/O	TTL	Flat 80pin	16I/32O for VME
O	TTL	Flat 80pin	1 for SUC
I/O	TTL	D-sub 25pin	1 for PC

Timing system using RTC

Figure 4 shows a block diagram of the timing system using the RTC.

A SUC outputs the frequency-divided clock to divide 508 MHz RF by 19488. This clock is the coincidence

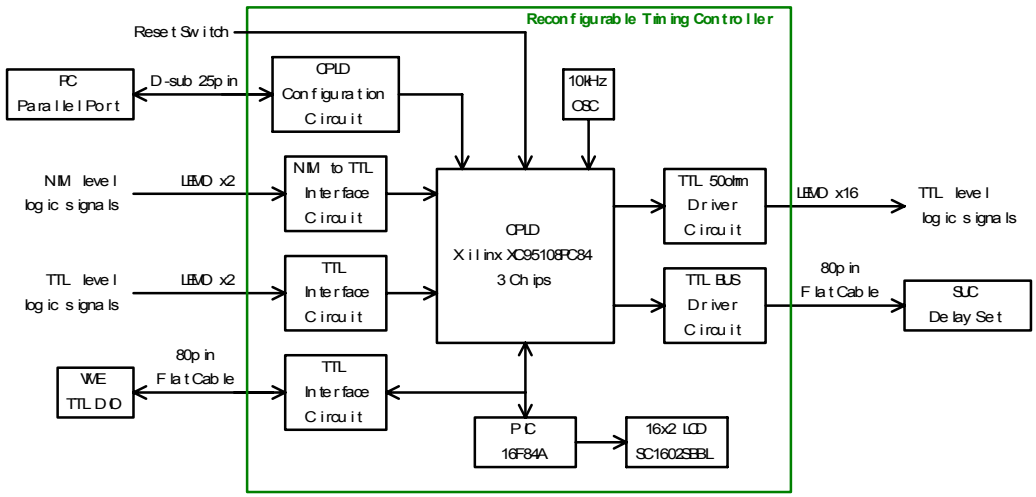

Figure 3: Block diagram of RTC and I/O interfaces to other devices.

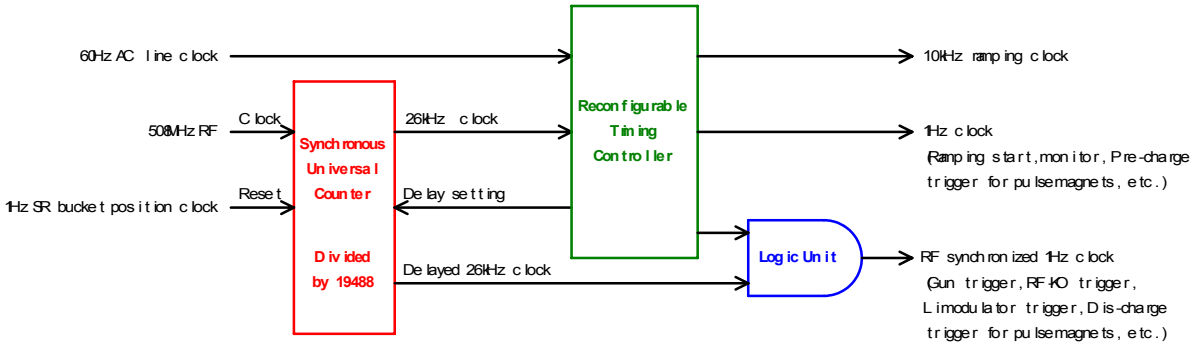

Figure 4: Block diagram of timing system using RTC.

clock between revolution clock of the booster and revolution clock of the storage ring. The number 19488 is the least common multiple of the harmonic number of 672 for booster and 2436 for storage ring. The CPLD in the RTC works by this clock. Linac modulator works synchronising with a 60 Hz AC line. We input a 60 Hz AC line clock to the RTC to synchronize output signals with it.

To shorten beam-filling time of the storage ring, the timing system has the function to inject an 8-pulse (max) beam from the linac into the booster and to inject into an RF bucket of the storage ring during one injection cycle of 1 Hz. The RF bucket position of the booster to inject electron beam is set as the delay of the coincidence clock. When we operate the 8-pulse injection, the RTC change the delay count of the SUC by eight times every 1/60 seconds.

Gun trigger is generated at logic unit module to coincide the delayed clock from the SUC with the gate signal from the RTC. Because the RTC works by the clock generated at the SUC, we can prepare the gate signal without any pulse-extend module and delay modules.

The RTC generate slow triggers. For example, it is the ramping start trigger, DCCT trigger to measure beam charge and BPM trigger to measure COD.

SOFTWARE

We used Xilinx free ISE WebPACK4.2 SP3 to program the logic in the CPLDs. The platform is Windows 2000. In the package, a schematic editor and a VHDL editor are prepared. We mainly used the schematic editor.

We use the VME TTL DIO board (HIMV-630 by NDS) for remote control of the RTC. Since we have already used this board in the SPring-8 control system, we could control the RTC by easy programming.

TOP-UP INJECTION

Top-up injection was planed to keep heat load of synchrotron radiation beam line equipment constant. Before, the operator started the electron beam injection by pushing “beam switch” button for radiation safety management. At the top-up injection, the time interval between the injections becomes short. It is necessary to modify the timing system to start the injection automatically using the information of stored electron beam current and elapsed time from previous injection and so on.

To realize it, the functions to start/stop the gun trigger, to count the number of already fired gun trigger, to enable/disable the injection and to read back the current settings are required to the timing system. We added these functions to the RTC. A GUI program running on the workstation at the central control room manages the sequence of the beam injection, and controls the RTC.

Test operation of the top-up injection has begun in September 2003. The RTC is well working important part in it.

CONCLUSION

We reconstructed our timing system using the RTC. Because of decrease of number of NIM modules, the timing system downsized. Since the modules, which the adjustment was necessary, had decreased, the maintenance of the timing system became easy. If new functions are requested to the timing system, then we can add these functions without increasing the modules.

REFERENCES

[1] N. Hosoda *et al.*, “Timing system of SPring-8 booster synchrotron”, ICALEPCS2001, San Jose, Nov. 2001.

[2] H. Suzuki *et al.*, “508.58 MHz synchronous universal counter for beam control system of SPring-8”, Nucl. Instr. And Meth. A431, (1999) p.294.