DIAMOND TIMING SYSTEM DEVELOPMENTS

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Abstract

The Diamond timing system is the next generation development of the design, principles and technologies currently implemented on the Advanced Photon Source and Swiss Light Source. It provides the features to distribute events, RF clock and time stamps over the same medium. To support the required level of precision for distributing timing fiducials and clocks, the transmission will use higher bit rates (at least 2.5 Gbps). It is currently envisaged that OM3 multimode fibre optic cable will be used as a medium. A new 4 channel timer module will be designed, with a resolution better than 20 ps, for systems which require fine time tuning. The timing system will be controlled through the Diamond distributed control system which is based on EPICS.

INTRODUCTION

Diamond is a 3rd generation, 3 GeV synchrotron light source currently being constructed in the UK. The storage ring is based on a 24-cell double bend achromatic lattice of 561m circumference. It uses a full energy booster synchrotron and linac for injection and will include an initial suite of seven photon beamlines.

A review of recent light source facilities and their timing systems [2] concluded that the timing systems developed for the Advanced Photon Source (APS) and the Swiss Light Source (SLS) [1, 2, 3] provided good functionality and performance together with integration to the accelerator control system based on EPICS. For these reasons, they have been adopted as the basis for the Diamond timing system.

PROPOSED REALIZATION OF DIAMOND TIMING SYSTEM

General Requirements

The timing system for Diamond is required to provide a means of generating and distributing timing fiducials to technical subsystems, in order to synchronize them to injection cycles and accelerating electron beams. To achieve this involves:

- The provision of reference signals and clocks, and their distribution to the technical subsystems with the required stability,
- Realisation of a reference time base (RF) to solve tasks of machine cycle control and synchronization to RF structure using a hardware of one type,
- A means for reference signal recovery at the destination points (RF clock) and time stability monitoring of timing signals globally,
- A time stamping mechanism for collected data and performed actions throughout the entire accelerator complex and beamlines,
- Integration into the control system to make synchronous actions in a distributed system.

Timing System Structure

The timing system will be structured with an event generator receiving the 500 MHz RF signal, triggers and other external signals. Timing events will be distributed over a network to multiple event receivers located in the control system interface layer, which then decode the events as hardware triggers or software interrupt requests. The triggers are connected to the equipment either directly or through timer boards clocked by the 500 MHz signal - as shown on Figure 1.

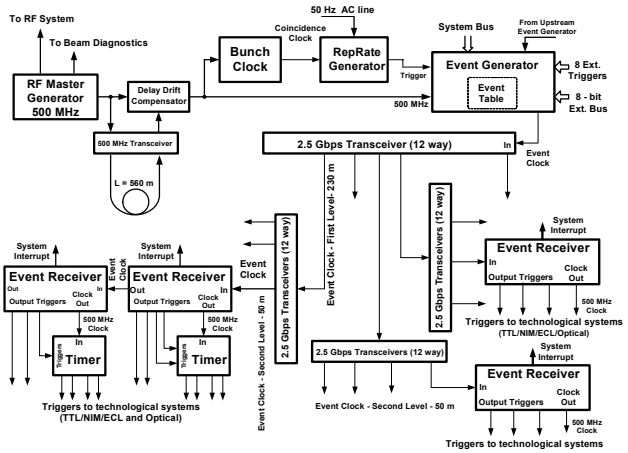

Figure 1: The Diamond timing system structure

Timing system network

The timing distribution network essentially defines the overall performance of the timing system. For Diamond the network has to deliver event messages to up to 250 event receivers in approximately 70 locations covering an area of 120000 m^2.

The requirements for the distribution network include:

- High transmission bit rate to minimize jitter,
- Compensation of thermally induced propagation delays,
- Simultaneous delivery of event messages to multiple destination points.

To realise these OM3 multimode fibre has been chosen as the transmission medium, operating with a bit rate of 2.5 Gbps over distances of 280 m. The network will be structured in a two-level multi-star topology, with retransmission nodes. The transceivers will operate at 850 nm using vertical cavity surface emitting lasers.

To confirm the performance of this choice, a number of test measurements have been conducted to verify the stability parameters of network components (transceivers, optical adaptors and cable). These tests used a WavePro7300 oscilloscope, a VS700 reference oscillator to produce a 625 MHz test signal, 2.5 Gbps transceivers from Infineon and Opticis and various OM3 multimode fibres of different lengths. Thermal effects were provided by a temperature-controlled enclosure with precision of 0.1°C over a range of 15°C to 50 °C.

Jitter Measurements

From the jitter measurements, similar to those shown in Fig.2, it is possible to conclude that the 2.5 Gbps Infineon and Opticis transceivers, V23818-N305-B57 and M3-250-LAT respectively, have the same stability. Each transceiver pair induces an RMS jitter of 0.7 ps, while a 350 m length OM3 fibre induces an RMS jitter of around 0.5 ps.

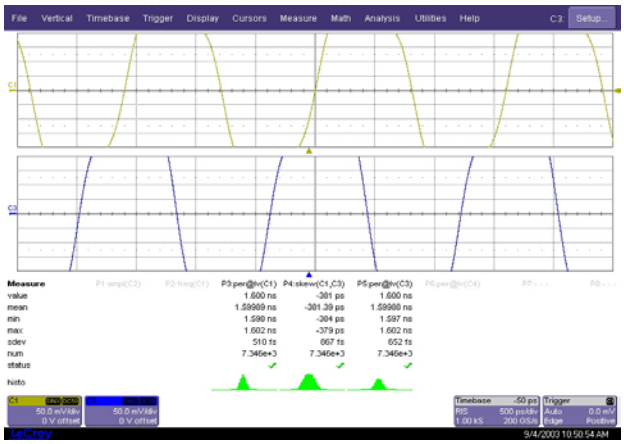

Figure 2: Jitter test of Infineon V23818-N305-B57 transceiver

Propagation Delay Tests

The change in propagation delay for OM3 fibre with temperature was measured over a temperature range of 17°C to 35 °C for a 700 m length. The results are shown in Figure 3, together with normalised values for 1 km and for the Diamond cable length of 280 m.

From these tests, the normalized differential delay drift of OM3 fibre varied from 60 to 65 ps/°C/km, compared with 74 ps/°C/km reported in [2] for OM2 multimode fibre. This gives a maximum change in propagation delay for the 280 m long cables of the Diamond network, and a temperature variation of 4°C, of 60 ps. This will be corrected on the Diamond timing system by a delay drift compensator module located between the RF source and the event generator, to reduce the error to a few picoseconds.

The differential errors on timing signal delivery to multiple destination points will minimized by equalizing the cable lengths with a precision of 2 - 3 m.

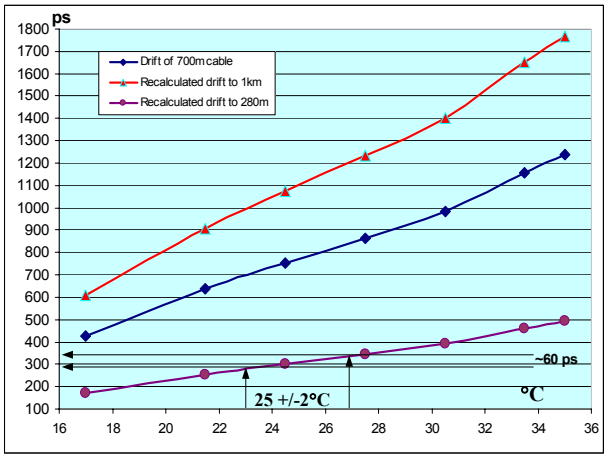

Figure 3: Propagation delay drift of OM3 fibre as a function of temperature

EVENT GENERATOR AND EVENT RECEIVER

A detailed functional description of event generators and receivers was given in [1, 3 and 4]. Diamond's timing system will maintain all of the functionality of the existing systems used in APS and SLS including register-level compatibility. Additional functionality will be implemented in the event receivers to perform jitter monitoring of decoded events and recovery of the RF-synchronized 500 MHz clock.

The jitter monitoring and RF clock recovery will be realized on two mezzanine cards which can be installed at locations that require these features.

Technical parameters of the event generator and receiver system are:

- Event message size	2 byte (with data of external distributed bus)
- Event message rate	up to 125 Mevent/s
- Event bit rate	2.5 Gbps
- Resolution of delayed pulses in event receiver	8 ns
- RMS jitter of:	
- decoded events	less than 20 ps
- recovered clocks	less than 5 ps
- IO ports	via interface cards
- System bus	VME64x
- Form factor	6U, single width

Jitter Monitoring

Within the event receiver optional hardware will be provided to undertake online jitter monitoring of the decoded events or clocks.

From any of selected events a delayed version of the signal is produced corresponding to allowable jitter, in the range from ten to hundreds of picoseconds with a resolution of 10 ps. The original event and the delayed version drive the clock inputs of two D-triggers which have their D inputs connected to an internal 125 MHz clock. The additional delay of the event should then

arrange the correct superposition of the jitter zone over the edge of the internal 125 MHz clock signal. Depending on the mutual superposition of the monitored signal and the internal clock signal, the logical combinations of the D-trigger's outputs can be interpreted as "jitter within range", "preceding jitter zone" and "following jitter zone". Three preset counters are then able to quantify the occurrence of these cases into values which can be used by the control system.

RF Clock Recovery

The recovery of the 500 MHz RF clock is provided by multiplying a 125 MHz clock, derived from the carrier clock, by a factor of 4 and processing it through commercial jitter cleaners.

FOUR-CHANNEL TIMER

A four-channel timer will be used in systems which require fine time tuning and low jitter of output pulses with respect to the accelerator RF. This timer will be realized by combining both counter-based and ECL transition effect principles according to the scheme on Figure 4. It will provide four independent channels consisting of a programmable clock divider (16 bit), a delay counter (16 bit), a pulse width counter (8 bit), a control gate, start/stop logic, an ECL-based D-trigger with a programmable delay (11 bit). The D-trigger will eliminate the jitter of FPGA-based counters, and whilst jitter performance of the final output pulses will be defined by ECL components.

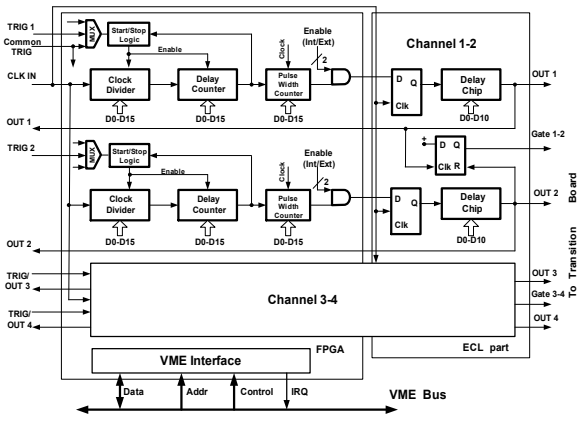

Figure 4: Functional scheme of the 4 Channel Timer

All timer channels will be able to operate either from an external clock signal, up to 500 MHz, or from an internal local oscillator (not shown on the diagram below). Triggers may be selected from a common trigger input, an individual trigger input, the output of another timer channel in a daisy chain arrangement, or a software command. Pairs of timer channels will be able to operate together to generate a "gate" signal whose length will be defined with a precision and stability of a few picoseconds.

Specification of the timer board (for 500 MHz clock):

Min. system delay	4 ns
Max. delay (1 channel)	8.589 s
Resolution	10 ps
Stability (RMS jitter)	1 ps (for ECL outputs)
Output pulse width	2 ns – 131 us
Inputs: - Clock	ECL (Front panel)
- Trigger	ECL/NIM (Front panel)
Outputs:	ECL (Front panel)
	NIM/TTL (Interface card)
System bus	VME64x
Form factor	6U, single width
Software support	EPICS

CONCLUSION

The structure and functionality of the Diamond timing system has been defined and represents an evolution of those of the APS and SLS. The measurements undertaken have shown that OM3 cable and transceivers from Infinion and Opticis are suitable for implementing the timing network. The developed set of modules should meet the functional and precision requirements of the Diamond timing system

ACKNOWLEDGEMENT

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