BEAM POSITION MONITORING USING INTELLIGENT FRONT-ENDS AND HIGH SPEED INTERCONNECT TECHNOLOGIES

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Abstract

Several recent technology advances enable innovative accelerator control and feedback system architectures. In this paper we show how these technology advances changed the rules. We take an all-in-one, single module solution intended for demanding beam position monitoring and feedback application as an example to illustrate our concepts.

INTRODUCTION

Recent technology advances are enabling development of a new class of accelerator and large experimental physics systems. Among the most prominent enabling technologies are: direct digitization of RF signals; high-speed field programmable gate arrays (FPGA) with embedded processors; high performance digital signal processing; high speed serial interconnect technologies; and embeddable middleware and application software technologies. We show that leveraging such technologies allows a different way of thinking when it comes to developing new systems. In this article we are suggesting a shift in perspective to reap the benefits of this situation.

The need for such a shift in perspective grows from our own experience with the development and system integration of beam instrumentation devices and observing the value of similar shifts in other industries like telecommunications. We chose a practical example to explain our ideas: Libera, a new product line. The first member is an all-in-one, feedback ready and customizable product. It is intended for demanding beam position monitoring and local and global feedback applications.

Our example illustrates the result of applying these ideas to a specific application. However, there is a much broader consequence of this situation. A common, reconfigurable hardware platform allows each user to customize various attributes of the system to its needs, yet at the same time benefit from the portability of the core all-in-one encapsulated software. Flexible software architecture allows rapid adaptation to multiple applications. By leveraging "commodity" technologies, this flexibility is actually achieved at reduced cost. The use of "open standards" for intra- and inter-system communication simplifies integration within the lab, and enables a broader view of integration between research facilities. This allows a higher level of collaboration among laboratories and industry. Our experience shows that this is a possible, creative and productive process.

ALL-IN-ONE

Digital Signal Processing Challenge

Direct digitization of IF or even RF signal allows functionality previously implemented in hardwired analog electronics to be implemented in digital electronics [1]. This evolution, where the boundary between analog an digital moves toward the sensor, requires tighter interactions between analog and digital sections. Examples of such interactions include closed loop mechanisms like gain control and carrier recovery. We call these interactions housekeeping. Standard modular crate solutions (VME, cPCI) in general partition hardware into analog, digital, DSP and CPU boards. This partitioning requires dedicated and expensive connectors and cables, which present a likely failure point. This means lower reliability and higher cost.

The model of "crate thinking" was a necessary and optimal approach in the past. But technology advances have changed the rules. Where well-defined boundaries between the implementation domains were once an advantage, they have now became a limitation. The all-in-one approach allows us to "fuzzy" the boundaries between the implementation domains. This allows the designer to concentrate on a functional decomposition of the design problem with fewer constraints. It also reduces the complexity of interconnections between implementation domains, as well as enables more optimal use of advancing technology. This in turn leads to a optimal, flexible, and cost effective implementation.

Timing Challenge

An analogous situation as with the closed loop control from the previous paragraph applies to timing signals that must span across different boards. An example of a timing synchronization challenge is a BPM system with digital signal processing, which requires tight synchronization between the DSP, digital and analog modules.

A robust, all-in-one solution, which encapsulates analog and digital hardware, sufficient processing power and fast serial interfaces seems a natural fit to this new reality [2].

Libera: An example of All-in-One Product Line

Libera is a new all-in-one product line. A single 1U high 19" enclosure contains analog and digital board with dedicated power supply.

The analog board is exchangeable, allowing multiple product line members to share a common digital board and enclosure. The analog board intended for BPM

applications implements four fast analog to digital converters for direct sampling of RF signal, on board low jitter VCXO and our unique (patent pending) technology to increase measurement accuracy and long-term stability.

The heart of the digital board is a powerful Virtex II Pro FPGA from Xilinx. In addition, there is a dedicated XScale® processor from Intel running Linux OS intended primarily for communication purposes.

Open architecture backed by substantial processing power makes Libera a powerful reconfigurable product. Figure 1 shows functional decomposition of a BPM processing implemented on Libera.

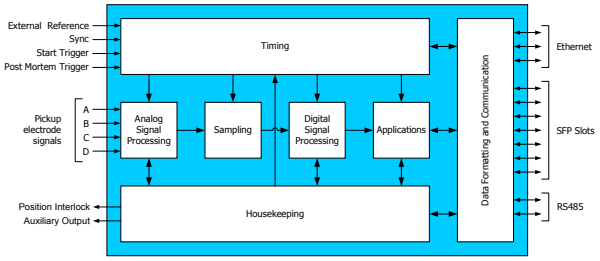

Figure 1: Libera functional diagram.

CONNECTIVITY

Fast serial interconnect technologies featured on Libera provide a brand-new perspective on the process of developing high-availability and next-generation accelerator control and feedback systems.

In general, individual modules may have their own processors, operating systems and memory and can communicate independently with other modules. Because nodes are operating-system agnostic, integration is no longer required at the driver/backplane level but ascends to the network and transport layers, using standard protocols, which means significant time savings and simpler design models.

Multi Tier Architectures

There is communication between elements of the beam position monitoring system (BPMS), as well as with the accelerator control system. There are several distinct types of communication, with different and conflicting needs. We have chosen multi-tiered network architecture. This allows each tier to be optimized for its particular purpose.

From the perspective of the BPMS, the communication requirements can be separated into two categories, public and private. These are relative terms. Public interfaces are with elements external to the BPMS, such as accelerator control system. Interfaces between the elements within the BPMS are termed private. The needs of each tier are very different.

Exchange of data between BPM nodes requires deterministic performance, high reliability and timely response. The concept of a private network means that the network topology is controlled, and so can be optimized to achieve the desired reliability and performance. In the Libera design, multiple Fiber Channel connections per node provide dedicated high bandwidth and connection redundancy. The connection topology may be optimized for each site by balancing redundancy with deployment cost. The private network is reliable, controlled and secure. It relies only on the lower two OSI layers to eliminate arbitration overhead.

The public network has different needs. It must be easy to deploy over a larger area and easy to interface with a variety of control system architectures. It is not possible to control the topology, from the BPMS perspective. Interfacing with external systems requires modest data rates and no demands for real time performance. Use of Ethernet and standard protocols (IP) makes deployment inexpensive and familiar.

The value of this division is that everyone can, with less compromise, select implementation strategy appropriate to his needs. This leads directly to reduced complexity.

For the purpose of this discussion, characteristics of Public include:

- Less controlled topology and thus less controlled performance;
- Greater flexibility required;
- Inherently “open” and so insecure;

And characteristics of Private include:

- Inherently “closed”, more secure;
- Dedicated bandwidth;
- Controlled topology, deterministic performance and redundancy
- Potentially less flexible

These are not absolute divisions, and there can be multiple levels of “public” and “private”. What is “public” (external) to the BPMS may be “private” within the lab, for example. This idea can be extend into more tiers with the same goal of optimizing network characteristics to the requirements at each tier. The terms “private” and “public” imply scope within a given context. There can be many levels of scope. If we think of tiers arranged vertically, “private” would imply a scope “below” the tier and public a scope “above” the tier. In other words, what is public to a lower tier is private to the tier above it.

If we attempted to achieve all communication via a single network tier, the conflicting requirements would lead to increased complexity, non-optimal compromises, and in general would have created a harder problem than necessary. By organizing into multiple tiers, it is simpler to implement optimal solutions.

Control and Data Flow

Within our communication model we can distinguish between control information and exchange of measurement data. This is a useful view as (again) the needs for each are different.

Achieving low latency and high data rates over the public interface presents a challenging problem. In contrast, the characteristics of our private network with controlled topology, high potential rates, and a provided

hardware coupling into the synchronized system, makes implementation of high rate, low latency communication much simpler. Fortunately we can partition our communication requirements so that we require only modest rates with no strict latency requirements over the public interface. We use the private interface for exchange of higher rate, time-critical data between BPM nodes.

Deterministic response implies that the timing of a control action can be determined precisely. It is important to realize that deterministic response is not the same as time-critical. Time critical implies specific maximum latency requirements. Deterministic does not necessarily mean time-critical.

Timing and Event Functionality

We have provided a synchronization mechanism, which can achieve a common time reference accurate in the range of nano-seconds. We use the concept of "scheduled events" to enable deterministic response, by specifying a dispatch time referenced to the common clock. This provides precise scheduled control where determinism is more critical than absolute latency.

The synchronization mechanism ensures that schedules have the same time quality on each tier in our communication model. We can achieve accurate signal timing at each level. At the lower level, we can achieve higher rates and lower latency; the higher level can have the same determinism, with lower rates of change.

CUSTOMIZATION

One of the key benefits of Libera is the opportunity to customize its functionality to specific applications, and within those applications to specific customer requirements.

The enabler for this customization is Libera's open architecture, built around the multi million gate Virtex-II Pro™ FPGA from Xilinx. This programmable device combines embedded processors (IBM PowerPC™ 405), with 3.125 Gbps transceivers. It addresses all existing connectivity requirements as well as emerging high-speed interface standards. Xilinx RocketIO™ transceivers offer a complete serial interface solution, supporting (among others) Fibre Channel, Infiniband, and 10 Gigabit Ethernet. Libera features 8 Small Form Pluggable (SFP) slots that can be equipped with customer selected copper or fiber transceivers.

For the purpose of this paper we identify three types of customization:

- Parametric customization allows adjustment of performance by simply changing parameters, without affecting architecture. Examples are analog board gain control and FIR filter bandwidth by changing tap settings.
- Architectural customization involves changes of logic configuration (FPGA firmware, DSP code and other software) to optimize performance for a particular purpose. It allows building specific logical and signal processing blocks, data-flow paths and algorithm implementations.
- The third customization involves communication interfaces: The Xilinx RocketIO™ transceivers together with the SFP interconnect form factor allow implementation of different communication standards without changing hardware.

Another important point is that the design flexibility supports assigning parts of the hardware so as to allow configuration of its functionality over the public network. Exactly which configuration changes are allowed now becomes a policy decision, not a technological issue.

CONCLUSIONS

We have presented a system design that expands the capability, performance and flexibility of our beam monitoring and control system significantly beyond prior expectations. We have employed "open system" concepts, leveraged standard communication protocols, and "commodity" technology to realize our goals.

Technically, this is achieved by applying recent advances in technology, such as high-speed sampling, fast high density FPGAs and advanced signal processing techniques. Enabling this design to become reality began by taking a different viewpoint on the problem, "thinking outside the crate". We examined the assumptions and facts that led us to the conventional "crate" solution. We realized that the rules have changed. Ultimately it was this fresh perspective that allowed us to view the problem more effectively.

The resulting architectural view identifies the characteristics of each part of the problem, and maps them effectively to design solutions. This shift in perspective is what allows us to identify the appropriate technology. The resulting system is only as complex as it needs to be.

The result has implications broader than we have demonstrated in this system. For example, the network architecture model we have used extends readily to a global scale, allowing us to question the boundaries of collaboration.

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