CTF3 BPM ACQUISITION SYSTEM

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Abstract

The CLIC Test Facility 3 (CTF3) is an R&D machine being built in order to validate concepts that will be used in the Compact LInear Collider (CLIC). CTF3 being an instrumentation intensive machine, considerable amount of money is put into the acquisition hardware and high quality cables used to bring the instrument signals to the digitalisation crates with as little degradation as possible. The main idea in this new approach is to reduce the distance between the signal source and the Analogue to Digital Converter (ADC) and therefore reduce the cost of the cabling. To achieve that, we have developed a radiation hard front-end that we install directly into the accelerator tunnel. This front-end deals with the digitalisation of the signals after an analogue buffering. Afterwards, the data is sent to a computer through the Serial Protocol for Experimental Control System (SPECS) field bus. Finally the digitalised signals are made available to the operation crew thanks to a device server implementing in FESA the OASIS interfaces. After a presentation of this low cost solution to Beam Position Monitor (BPM) acquisition, the paper gives the results of the first integration tests performed in the CTF3 machine.

OVERVIEW

The CLIC Test Facility 3 (CTF3) is a R&D machine being built at CERN to validate concepts that will be used in the future CLIC (Compact LInear Collider) such as the two-beam acceleration scheme. Beam instrumentation is very important in such a machine and, although the machine is small compared to the other CERN's accelerators, we have several hundred ADC channels acquiring beam position monitors, wall current monitors, and other instruments. The ADCs are usually concentrated in few VME crates installed outside the radioactive areas and cables are pulled to bring the signals from the sources to the digitisers. To reduce to the minimum the signal degradation, high quality cables are used. A rapid computation shows that, with this scheme, quite an important amount of money is invested in kilometres of high quality cables.

With cost reduction in mind, a new BPM acquisition system was proposed and is being developed in a collaboration between CERN and LAPP. The breakthrough of this system is to move the digitalisation part from the VME crates down to the accelerator tunnel replacing the expensive high-quality cables with cheaper Ethernet cables.

The rest of the paper is structured as follows. The next section presents the system architecture showing the main components and how they interact. The subsequent sections detail the internals of the various parts. Finally, test results and the installation plans are given.

ARCHITECTURE

The system is made of four parts as depicted on figure 1. At the bottom, we have the instrument that produces the signals we want to digitalise, e.g. a BPM. The analogue signals are connected to the front-end that is installed very close to the instrument (typically 10 meters) in the radioactive zone. On trigger reception, the front-end buffers the data in analogue form using an analogue memory and converts it with a slower but radiation hard ADC. Once digitalised, the data is read from the front-end memory by a gateway using the Serial Protocol for Experimental Control System (SPECS) field bus. Since the gateway is not radiation hard, we install it in a technical building outside the machine tunnel.

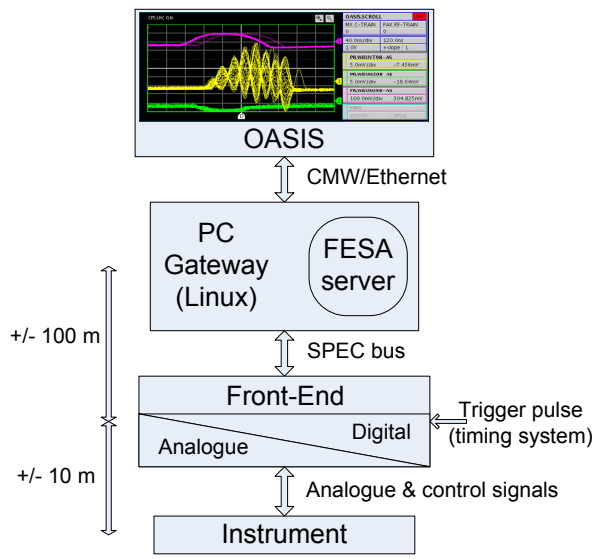

Figure 1: System architecture.

The front-end is connected to the gateway using plain category 6 Ethernet cables running on distance of typically 100 meters. The acquired waveforms are exported into the control system by a device server written with the CERN Front-End Software Architecture (FESA) framework. The server implements the properties specified by Open Analogue Signal Information System (OASIS)[1]. Thanks to the Scope & Channel interfaces, the system is directly connected to the OASIS application server that manages the connections and the acquisition settings. The physicists working in the control room have access to the signals using either the OASIS generic viewer or dedicated applications based on the OASIS client library.

FRONT-END

The Front-End consists of two parts: the analogue front-end connected to the beam position monitor for signal amplification and calibration and the digital front-end (DFE) to digitalise and send the data to the gateway. Up to six DFEs are grouped together under the beam pipe inside a chassis with a distribution board. The DFE receives the differential signals conditioned by the analogue front-end. On trigger, the analogue memories sample the signals at 512 MS/s with a dynamic range of 12 bits. Once the memories are filled up, they are read out at 800 kHz by a bipolar 14-bit ADC. This acquisition cycle must be executed between two beam pulses. The digitalised data is stored in the internal RAM of the FPGA. A SPECS mezzanine is plugged on each DFE for the transmission between the front-end and the gateway.

With the four electrodes' signals from the BPM, the analogue board produces three signals: a sum (∑) and two differences (ΔH & ΔV). Depending on the BPM's type, these differences can be either the horizontal and vertical deviations or the two diagonal deviations. A final calculation is done by software in the gateway to have normalized horizontal and vertical deviation signals.

The reason why we have chosen the solution of the fast analogue memory and a slower ADC is to resist the radiations and be able to install the system close to the beam (cable cost minimisation). All the components have been chosen to resist at least 35 kRad. The analogue memory is a SAM (Swift Analogue Memory) developed by Commissariat à l'Energie Atomique (CEA). The ADC, a LTC1419 from Linear Technology, matches the memories characteristics, 14-bit resolution and differential inputs, and is fast enough to read the SAM content between two beam pulses.

For the data transmission, the mezzanine is connected to the FPGA through a parallel bus. As on the DFE, the FPGA on the SPECS mezzanine is an ACTEL ProASICPlus. It is a flash FPGA which has also been tested and resists up to 35 kRad.

An additional feature of the digital front-end is the analogue board control. Gain, attenuation and calibration are configured through the digital board with the SPECS bus. A control signal to select which BPM to calibrate is sent by each DFE to the distribution board. A small logic bloc on the latter is implemented to send the calibration pulse to the right BPM. The distribution board is also used to receive and amplify signals such as the main sampling clock from the RF system and the beam synchronised trigger. At last, it serves as a power supply distribution for the digital front-end boards.

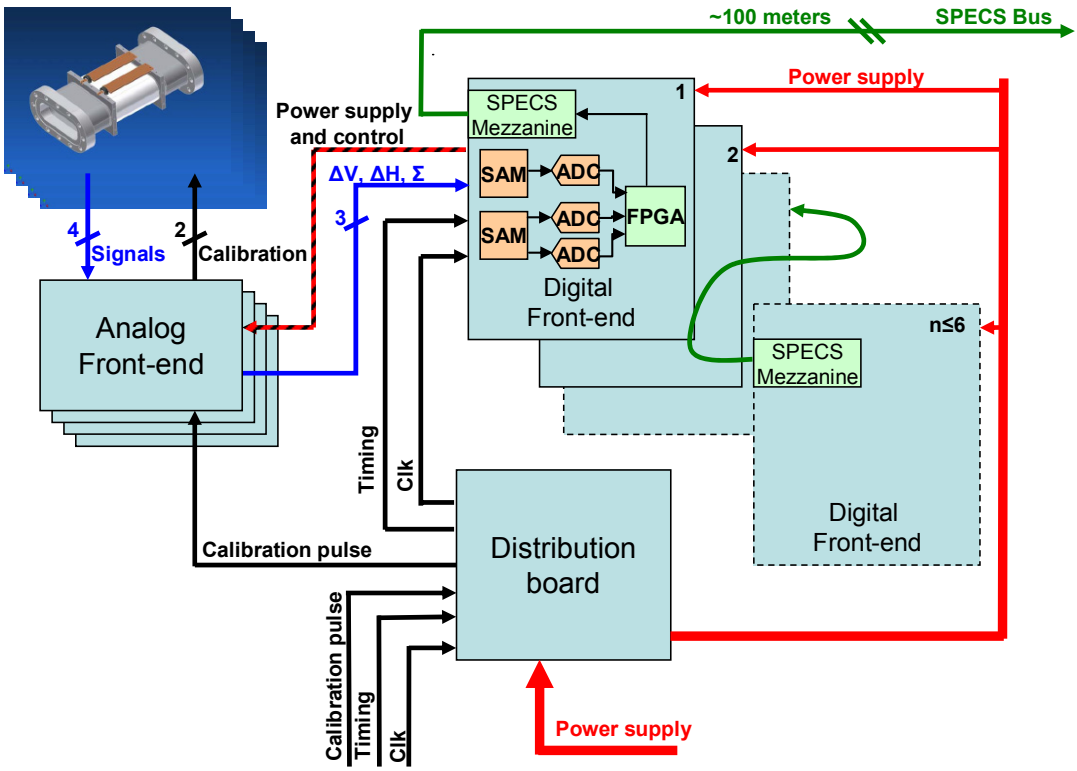

Figure 2: Hardware configuration.

SPECS BUS

The SPECS (Serial Protocol for Experimental Control System) was developed initially for LHCb sub-detector electronics [2]. It is used for front-end control and read out from control room. It consists of a master PCI board in a gateway far from radiation and a slave mezzanine near the beam or detector. They are connected by an Ethernet cable. The maximum distance between them is 130 meters. The protocol used is not Ethernet but a home

made protocol with BLVDS levels. It consists of four twisted pairs, two for transmission and two for reception, with one pair dedicated to the data and one to the clock. The clock runs at a frequency of 40 MHz.

The mezzanine can be connected to a mother board through a parallel bus, I2C bus or JTAG. On the digital front-end board we use the parallel bus. There are 16 bits for the data, 8 for the address and, 5 for control. One channel for the 40 MHz clock is also available. The bus has a data rate of 1MB/s.

One PCI master board can drive up to four SPECS buses and it is possible to chain up to 9 mezzanines on the same bus. It means 4 to 36 slaves can be connected on one PCI master board. This is a good solution, provided the data rate is sufficient, to reduce the number of cables and gateways. It allows us to reduce further the cost of the system. Tests have validated a configuration with nine mezzanines chained together.

Software wise, a complete set of libraries and drivers is available and can be used to adapt the SPECS to other systems.

GATEWAY

The gateway is a standard rack-mountable PC running Scientific Linux CERN 4. The mother board has 3 PCI slots. One PCI slot is reserved for the timing receiver and the other two are used for the SPECS Master cards.

After digitalisation of the signals by the DFEs, the acquired data is retrieved by the gateway, normalised according to the BPM type and transferred to the OASIS application server.

A library has been developed to communicate with the front-ends, via the SPECS parallel bus. This library is based on the SPECS library and driver. In addition to the data retrieval, the communication link is also used to configure the front-ends.

To implement the OASIS interface [3], two classes, LappBPMScope and LappBPMChannel, have been developed using the FESA framework [4]. They manage respectively the front-ends and the channels along with their properties. Both classes are deployed in a FESA server that processes the requests from the OASIS application server. The timing pulse used to trigger the DFEs is also linked to a FESA real-time action. This action updates the acquired values in the LappBPMChannel instances and initiates the transfer to the OASIS system.

TEST RESULTS & INSTALLATION

Tests with beam were carried out during last spring with one DFE. A complete hardware chain, from the BPM to the Linux Gateway, was used. Simplified software was used to control the two front-end boards and to read and display the acquired data.

We successfully read acquired signals and computed beam positions. We controlled the analogue front-end's settings from the control room. The tests also validated SPECS transmission with a 130 meter long Ethernet cable – the longest foreseen in our installation. At last, there was no problem due to radiation effects on the electronic.

It is planned to install around 50 digital front-end boards in the CTF3 second transfer line (TL2) and the Experimental Area (CLEX) starting the first semester of 2008. We have decided to connect up to 6 digital front-ends per SPECS bus. Since there are 3 PCI slots in every PC gateway (one for the timing receiver and two for the SPECS master boards), we need only 2 gateways and 9 long Ethernet cables.

CONCLUSIONS

The first tests have validated the first DFE prototype as well as the whole system. The second DFE prototype is being tested before launching the final series.

An installation for 50 BPMs with the original solution (ADCs in VME crates and long HQ cables to bring the analogue signals) would cost about 240 k€. With the DFE solution, the total cost is around 80 k€ including the PC gateways, SPECS boards, the DFEs and the cables (power supply, calibration and, SPECS buses). That means the new solution is three times cheaper! In fact, in addition to the significant cost reduction, we have also improved the acquisition chain. With the digitalisation closer to the source, we have a better signal/noise ratio and the analogue memory/14-bit ADC combination has a higher effective number of bits.

The DFEs will also be used to acquire instruments other than the BPMs, which the system was initially designed for. Furthermore, with a constant cabling cost reduction in mind, we are also investigating the possibility to include the calibration system and the power supply inside the front-end chassis. The final goal is to have an autonomous chassis directly connected to the mains.

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