DEVELOPMENT OF
FLEXIBLE AND LOGIC-RECONFIGURABLE VME BOARDS

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Abstract

We developed logic-reconfigurable VME boards with high flexibility. The board has two parts, a base board and two I/O daughter boards. The base board has a field-programmable gate array (FPGA) chip for the execution of user logic, such as a digital low-pass filter or the calculation of the center of a spot image. Users can install their logic into the FPGA via the VME bus. The I/O daughter boards are simple I/O modules such as analog inputs and outputs (AI/AOs) or digital inputs/outputs (DIOs). The data from the I/O board is sent to the base board and processed there. As the I/O module is separated physically, the user can customize the VME board by choosing I/O modules and does not need to develop the whole device. We have developed DIO, AI/AO and camera link interface modules [1] as I/O daughter boards.

INTRODUCTION

Software on a CPU and simple AI/AOs and DIOs enables us to build control systems with complex sequences, such as feedback routines. However, a fast sequence that requires sub-100-microsecond-order timing is currently impossible to achieve by software on a CPU. Hardware in the form of a hard-wired circuit, on the other hand, provides control of fast sequences. However, the hardware sometimes has limited flexibility and requires considerable time and cost to adjust the sequence.

We developed an I/O flexible and logic-reconfigurable board that enables both the control and adjustment of fast sequences. The design concepts are discussed in section 2, and the specifications are given in section 3. We present examples of potential applications of the new board in section 4. Finally, we conclude our study in section 5.

DESIGN CONCEPTS

We adopted three main design concepts. These are (1) flexible I/O selection, (2) real-time and fast control, and (3) sequence reconfigurability.

Flexible I/O Selection

We separated I/O parts physically from the base board. The I/O parts are simple I/O modules such as an AI/AO or DIO module. Two I/O parts can be installed on the base board as daughter boards (see Fig. 1). They are connected to the base board by three 64-pin connectors. The data from the I/O board is sent to the base board through the connectors. All the data processing for the sequence is performed on the base board.

The users can choose appropriate I/O daughter boards

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for their own system and develop the logic of the sequences to be carried out. If the specifications of the existing I/O daughter board do not fit the user's system, the user only needs to develop a simple I/O module. The same base board can be used with different I/Os with a small modification of the logic and without any modification of the hardware, such as a printed circuit board design. This design concept provides high flexibility for I/Os and shortens the hardware development time.

Figure 1: A photograph of the flexible and logic-reconfigurable VME board mounted with DIO (left side) and camera link grabber (right side) daughter boards. The user FPGA (lower) and bus-control FPGA (upper) are mounted in the middle of the base board.

Real-time and Fast Control

The base board is mounted with FPGA chips. The user sequences are on one FPGA chip with 1.5M gates. The FPGA execute user logic at a base clock frequency of 32 MHz. The FPGA enables real-time and fast control with microsecond-order response, which software on a CPU at present cannot achieve.

Sequence Reconfigurability

We adopted the FPGA because it is reprogrammable. The development of a system with complex sequences often needs adjustments. The FPGA enables both reprogramming the sequence and testing the sequence with the actual equipment being controlled in the same place, because changing the logic in the FPGA only requires the modification of configuration data.

The feature of reconfigurability also enables us to carry out R&D for the sequence because of the easiness of logic modification. The users can test several sequences to find
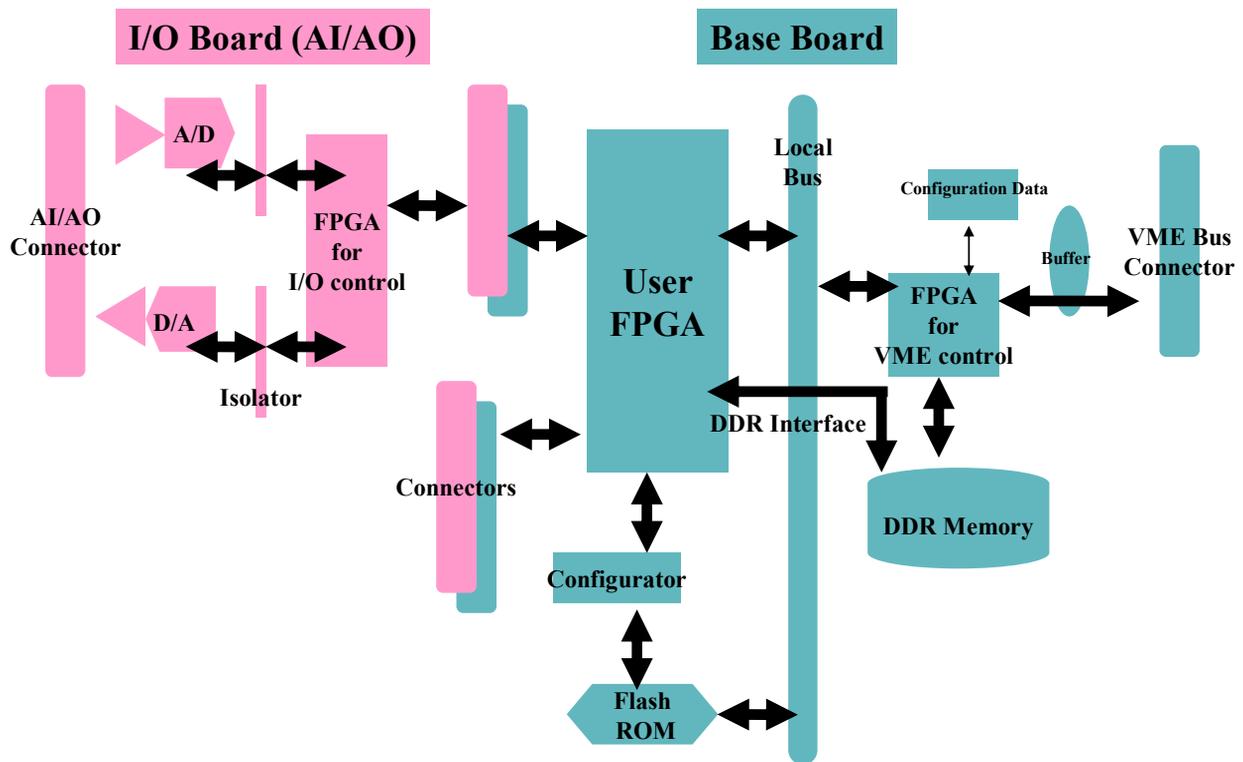
Figure 2: A block diagram of the flexible and logic-reconfigurable VME board. Green blocks are elements on the base board and pink blocks are elements on the I/O daughter board.

the appropriate one for their equipment in a short period of time.

The configuration data of the FPGA is stored in a 64 MB Flash ROM on the base board. The configuration data can be uploaded from a CPU through the VME bus. This makes reconfiguration easy.

In addition to the three design concepts, we add several features to the board.

The bus of the board is the VME bus. We adopted the VME bus because the existing control system in SPring-8 [2] is mainly built on the VME system.

We designed the base board to have two FPGA chips. One is for the user sequences and the other is for the bus control. The logic for the bus control is separated from that of the user. A different bus can be adopted by modifying the logic in the FPGA for bus control. The logic of the user is not affected by a change in the bus.

A double-data-rate (DDR) memory chip is also mounted on the board. The DDR memory is used as temporal data storage. The board can execute sequences that require a large amount of memory.

The logic for memory access is in the VME-bus control FPGA. The user FPGA is equipped with an interface for the DDR memory, which is directly connected to the VME-bus control FPGA. This design avoids a "collapse" of the logic for the memory access while compiling user logic.

Data in registers of the FPGA and the DDR memory are mapped as VME A32 registers. The user can access the

Table 1: Specifications of the flexible and logic-reconfigurable VME board

Base board	
User FPGA	Xilinx Spartan3 XC3S1500
Number of I/O module	2
Memory	256 MB DDR memory
Bus	VME revision C.3
I/O daughter board (AI/AO)	
Number of channels	AD: 8 ch, DA: 8 ch
Bit resolution	16 bits
Sampling rate	200 kHz
I/O daughter board (DIO)	
Number of channels	DIO 96 ch
Signal level	TTL
I/O daughter board (Camera link)	
Number of channels	Camera link: 1 ch External trigger: 1ch NTSC output: 1ch
Configuration type	Base configuration
Supported camera	IPX-VGA210-LMCN (Imperx Inc.)

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data from the CPU with a simple VME I/O control function.

SPECIFICATIONS

The new flexible and logic-reconfigurable VME board was developed in cooperation with ARKUS Inc. [3]. All the design concepts were implemented. Figure 2 shows a block diagram of the board. We developed three types of the I/O daughter boards. They are the AI/AO, DIO, and camera link grabber. The specifications of the base and the I/O daughter boards are shown in Table 1.

APPLICATIONS

PID Feedback System

A proportional-integral-derivative (PID) feedback system is an application of the new board. A base board with the logic for a PID feedback sequence and an AI/AO daughter board function as the feedback system.

The system is intended to be installed as a replacement for the existing monochromator stabilizer (MOSTAB) of a beamline of SPring-8 [4], [5], which was developed on custom-built hardware. An analog signal from an intensity monitor is fed to the I/O of the new board and the result of the logic is converted to an analog output. The logic includes a low-pass filter and a PID sequence. The output is fed to a piezo actuator in the monochromator to adjust the beam position.

We tested the feedback system with pulse width modulation (PWM) output instead of analog output. The test system is a magnet system that requires PWM control at a frequency of 1 kHz. For this test system, we added a DIO daughter board and logic that converts the result of feedback to the PWM control unit. No hardware modification was needed. The test shows the flexibility of the new board. The test system worked well and the MOSTAB system with the new board is ready for installation.

Screen Monitor System

Another application of the new board is a beam position screen monitor system [6]. An image of synchrotron radiation on a screen is captured by a camera with a camera link interface. The system must calculate the relative intensity and the center of the beam spot from the image. The image of the camera has the following specifications: 200 fps, 640×480 pixels, and 12 bits/pixel. The system is also required to collect 8 analog signals from detectors. The system can be built with the new board. The board needs logic for image processing on the base board and two I/O daughter boards, namely, the camera link grabber and AI/AO boards. The image data is stored in the DDR memory. We will install this system with a new screen monitor in March 2008.

CONCLUSION

We designed and developed a new VME board that is characterized by flexible I/O selection, real-time and fast control, and sequence reconfigurability. We applied the board to a PID feedback system and plan to apply it to a system for a screen monitor. No hardware change was required to apply the systems.

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