STATUS OF THE LHC POWER CONVERTER CONTROLS

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Abstract

The LHC has more than 1700 power converters spread around the 27 km machine. Controlling them all is an unprecedented challenge due to the part-per-million level accuracy required for the main circuits and because the majority of the systems are exposed to significant levels of radiation. The project began in 1996 and has consumed 7 MSF and around 50 man years. The architecture chosen is similar to the one used successfully in LEP with one embedded controller per power converter linked by fieldbuses to middle-tier gateway systems. This paper presents a summary of the architecture and the results achieved during the commissioning of the LHC from 2006-8. The system contains numerous enhancements compared to LEP including: digital regulation of current; automatic configuration based on a machine readable inventory; extensive remote diagnostics of power converter and controller faults; and distribution of time of day, timing events, software updates and power cycle requests over the WorldFIP fieldbus.

OVERVIEW

All magnet circuit power converters in the LHC are current sources. They are formed by integrating a voltage source, a current measurement system and a Function Generator/Controller (FGC). The FGC has a WorldFIP interface and up to 30 are connected per fieldbus segment to a gateway. Figure 1 shows an overview of the converter controls architecture [1].

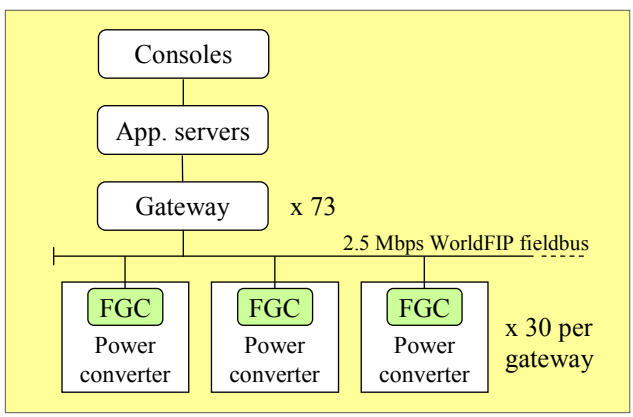

Figure 1: LHC Architecture overview.

The gateways are situated in 8 surface buildings around the LHC, with roughly 10 per building. The vast majority of the power converters are underground with 750 actually in the LHC tunnel. Gateways are rack mounted diskless x86 Linux PCs. They run a dedicated program that links the LHC technical Ethernet with a 2.5Mbps WorldFIP segment. The gateways relay commands and responses between applications and FGCs and also support links to general services such as alarms, logging and post mortem.

FUNCTION GENERATOR/CONTROLLER

The FGC is an embedded computer with analogue and digital I/Os dedicated to controlling LHC power converters. Development began in 1996 [2] and a prototype was running by 1999 [3]. The final design was prepared in 2001 [4] and produced from 2003 to 2005 [5].

Physically an FGC is an assembly of six small printed circuit boards (PCBs) mounted on a motherboard enclosed in a metal cassette with dimensions 6U x 20TE x 170mm (see figure 2). The PCBs have the following functions:

1. WorldFIP and RS232 interfaces, Dallas 1-wire bus driver, front panel LEDs and push buttons
2. M68HC16Z1 Microcontroller (MCU) and TMS320C32 Digital Signal Processor (DSP)
3. Error corrected memories for MCU and DSP
4. Digital I/O interface (8 commands, 16 status)
5. Analogue I/O interface (2 ADCs, 1 DAC)
6. Interlock and diagnostic interfaces

This separation will allow the redesign and replacement of a part of the system should this become necessary. From the start, two different analogue I/O interfaces have been produced, one for the use in the LHC tunnel where radiation levels are significant, and one for other areas.

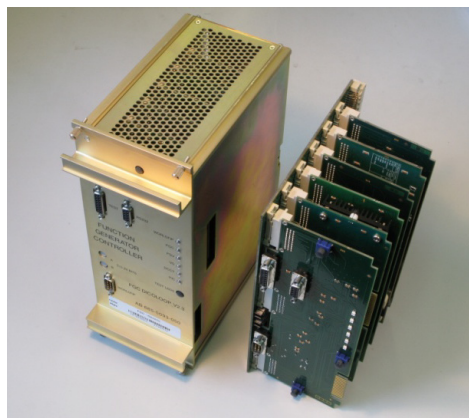

Figure 2: FGC hardware, with and without its cassette.

A metal cassette is used to protect the PCBs and to make the FGC a closed module that can be replaced by the standby service in the event of a failure. Cassettes can be stacked and several have survived being dropped. There are no user adjustable elements of any sort.

The software in the FGC has become extremely sophisticated. There is a boot program responsible for self-tests and software updates and a main program that provides the functionality for controlling an LHC power converter. A huge effort was put into making the system

maintainable, given that more than 1700 FGCs must be managed. Numerous aspects of the global FGC system are defined in XML files which are parsed by a perl script to create C header files and documentation web pages (currently more than 2500 are generated). The FGC manifests more than 400 properties, the majority of which are concerned with system diagnostics.

ELECTRONICS CRATE

Interconnections are always a potential source of unreliability as well as being expensive to assemble and test, so a new method for making FGC crate backplanes was developed that requires no wiring. Using a rigid 3.2 mm thick PCB it is possible to mount DIN 41612 Type C connectors on one side (for the FGC, PSU, etc...) and Burndy connecters on the other (see figure 3).

Figure 3: A wiring free FGC crate.

This technique has proven to be extremely successful and has been adopted by other LHC equipment groups.

RADIATION

It was decided early in the LHC design to place the orbit corrector magnet power converters in the LHC tunnel under the cryostat. This saved a huge amount in cabling and in the size of the power converters, however all devices in the tunnel must tolerate a fluence of ~10^{10} particle/cm^2/year (E>20MeV). Some steps were taken to try to make the power converters survive this fluence including over-rating the power switching components.

Early radiation tests of the prototype FGC showed that memory corruptions are inevitable and so error detection and correction devices were added. RAM based programmable logic was avoided and instead, flash based Xilinx CPLDs were used throughout. These have been shown to be fairly robust but early tests in a 60MeV cyclotron now appear to have underestimated the cross section for single event latch-ups with higher energy particles. Further tests are underway, but the success of this solution is not certain once the LHC reaches its design luminosity.

It was thought in the beginning that non-tunnel areas would be free from radiation, so no effort was made to make other types of power converter tolerant. The FGCs in these areas use a higher performance analogue interface that uses an SRAM based FPGA to implement a digital filter. Simulations now show that significant radiation levels (especially neutrons) will be present in many underground areas and the reliability of the converters and FGCs is a concern. A new analogue interface is being tested that does not use an FPGA and other mitigation methods will be implemented, however the eventual failure rate may still be a problem. A crash program to develop a new variant of the FGC based on more robust components is under consideration. A similar study is looking at the voltage sources.

FUNCTION GENERATION

The floating point DSP is responsible for calculating the current reference in real-time. This can be defined as a linearly interpolated table of current against time or parametrically in the form of parabolic, linear and exponential segments. Sine wave, square wave and step functions are also supported for testing purposes.

Real-time control is possible using a 50 Hz data channel via the fieldbus and this will be used for orbit, tune and chromaticity feedback. The real-time channel can either directly define the current reference, or an offset from the pre-loaded function.

CURRENT REGULATION

The regulation of the measured current uses a control algorithm based on the RST tri-polynomial form in which the performance of the regulation (R, S) and tracking (T) can be independently optimized [6] (see figure 4). The polynomials are calculated to match an inductive load with parallel and series resistances and to implement a proportional-integral-integral controller (PII).

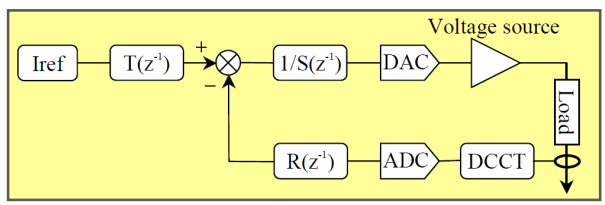

Figure 4: Overview of the current regulation.

As a result, R(z^{-1}) has three coefficients, S(z^{-1}) has four and T(z^{-1}) five. An algorithm for calculating R, S and T is included in the DSP so the user can enter the circuit parameters and the desired closed loop bandwidth.

The small signal bandwidth for LHC circuits is in the range 0.1 Hz to 5 Hz. The RST algorithm is typically run 10 times faster than this. The ADC is always sampled at 1 kHz so that the measurement can be filtered digitally to remove 50 Hz noise.

The RST algorithm has excellent tracking and in combination with the high quality current measurements it has been possible to meet the demanding accuracy requirements for the main LHC circuits. Tracking tests between the main circuits in one LHC sector showed an error of less than 2 ppm during the whole ramp.

WORLDFIP COMMUNICATION

WorldFIP was the chosen fieldbus for the LHC power converter controls and for many other types of equipment because it offered several unique features:

- Deterministic traffic (5µs max jitter)
- Periodic fixed length packets (up to 64 bytes)
- Aperiodic variable length packets (up to 128 bytes)
- Radiation tolerant chipset (no longer produced)

The main weakness is the limited bandwidth. The bus runs at 2.5 Mbps, but real throughput is limited to about 1 Mbps because of the real-time protocol. WorldFIP operates in a cyclic way with the start of each cycle triggered by an LHC timing receiver signal. For the FGCs the cycle frequency is 50 Hz and every cycle starts with the broadcast by the gateway of a 64 byte packet containing the UTC time and timing events (if any). The time of arrival of this packet is used to discipline a phase locked loop in each FGC [7]. In each cycle there is a time window of 7 ms dedicated to aperiodic variable length packets. These are used for commands and responses and allow the gateway to communicate with all 30 FGCs at the same time. This parallelism means that despite the modest throughput to any one FGC, an application can send commands to all 1700 simultaneously which results in very good system level performance (e.g. 120 ms for a command of less than 120 bytes).

CONFIGURATION AND INVENTORY

An objective for the FGC system was that no adjustments should be required when an FGC is replaced. To make this possible an automatic configuration system was developed [8]. Configuration properties are divided into three groups: *system* properties, *equipment* properties and *type* properties. System properties are associated with the name of the power converter (e.g. circuit resistance) while equipment properties are associated with an individual asset (e.g. ADC gain). Type properties are associated with the type of equipment (e.g. voltage source gain).

So for equipment and type properties the individual assets must be identifiable and this is done using Dallas 1-wire devices (DS2401 or DS18B20). Nearly 40,000 of these devices have been embedded in assets enabling automatic configuration and an online inventory to be compiled. All analogue measurement assets (ADCs and DCCTs) use the DS18B20 device which also measures the temperature, enabling improved circuit current measurement accuracy [9] as well as environment and ventilation monitoring.

LESSONS LEARNED

- If there is any way to avoid radiation then do so. Designing radiation tolerant electronics is a huge challenge and should be a solution of last resort.
- Any large scale control system must have scalability designed in from the start. Parallelism in the communications is vital but actually only helpful if asynchronous commands can be sent by the applications.
- Only add diagnostics if they are sure to be much more reliable that the thing they are monitoring. For example, the FGCs can measure their power supply voltages, but most reported failures have been due to the measurement electronics rather than the power supplies.
- The control algorithm in an embedded digital controller is only a tiny part of the software. The main part will concern the mundane but essential tasks such as command parsing, error handling, logging and diagnostics.

SUMMARY

The evolution of the proven LEP architecture for the LHC has been successful although the radiation tolerance of the design is still to be seen in practice. The modular nature of the FGCs provides a physically and electrically robust controls solution and automatic configuration is particularly valuable as it reduces the chance of human error during an intervention.

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REFERENCES

[1] S. Page, “Integration of the LHC power converters within the high-level LHC control system”, ICALEPCS’05, PO1.043-6

[2] J. G. Pett et al, “A strategy for controlling the LHC magnet currents”, EPAC’96 p.2317

[3] Q. King et al, “Developments in the High Precision Control of Magnet Currents for LHC”, PAC’99 p. 3743

[4] Q. King et al, “The All-Digital approach to LHC power converter current control”, ICALEPCS’01, THBT004

[5] P. Fraboulet, “Application of advanced hardware testing and inventory management methods for the LHC power converter control system”, ICALEPCS’05, PO2.038-3

[6] F. Bordry, H. Thiesen, “RST Digital Algorithm for controlling the LHC magnet current”, CERN/LHC Project report 258

[7] Q. King, “Advanced uses of the WorldFIP fieldbus for diverse communications applications within the LHC power converter control system”, ICALEPCS’05, WE4B.3-2O

[8] S. Page et al, “Automatic inventory and configuration management tools for the LHC power converter controls”, ICALEPCS’09, TUA004

[9] M. Bastos et al, “Developments in High-Precision aspects of power converter control for LHC”, PAC’07, MOPAN070