DEVELOPMENT OF A FPGA BASED RF CONTROL SYSTEM FOR THE S-DALINAC*

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Abstract

The Superconducting DArmstadt electron LINear ACcelerator S-DALINAC has a maximum energy of 130 MeV and beam currents of up to 60 µA. To reach this energy conveniently in cw superconducting cavities with a high Q at a frequency of 3 GHz are used. In order to achieve a minimum energy spread, the amplitude and phase of the cavities have to be controlled strictly in order to compensate the impact of microphonic perturbations. The existing analogue RF control system based on a self exited loop, converts the 3 GHz signals down to the base band. This concept will also be followed by the new digital system currently under design. It is based on a FPGA in the low frequency part, giving a great flexibility in the control algorithm and providing additional diagnostics. The low level RF system is controlled via CAN bus. We will report on the design concept, the status and the latest results measured with a prototype.

INTRODUCTION

The Superconducting DArmstadt electron LINear ACcelerator S-DALINAC [1] is a recirculating linac, which is shown in Fig. 1. Since its first operation in 1987 it is used as a source for astro- and nuclear physics experiments with beam currents of up to 60 µA and a maximum energy of 130 MeV, which can be reached if the beam is recirculated twice. In order to reach the energy superconducting (sc) 2 cell, 5 cell and 20 cell niobium cavities are used. The operating temperature of these cavities is 2 K. The design quality factor Q is $3{\cdot}10^9$ at an accelerating gradient of 5 MV/m and a frequency of 3 GHz. Even when the sc cavities are strongly coupled with a loaded quality factor of $3{\cdot}10^7$, which leads to a resonance width of some 100 Hz, they are very sensitive against microphonic perturbations. The impact of these perturbations has to be compensated by a low level RF control system. This system has to control the amplitude and phase of the cavities strictly in order to minimize the energy spread to $\pm1{\cdot}10^{-4}$ at the experimental areas. The stability specification for the amplitude and the phase needed to fulfil this recommendation are given in Table 1.

Table 1: Stability Specifications

Relative amplitude stability	ΔE/E	$\pm8{\cdot}10^{-5}$
Phase stability	Δφ	±0.7°

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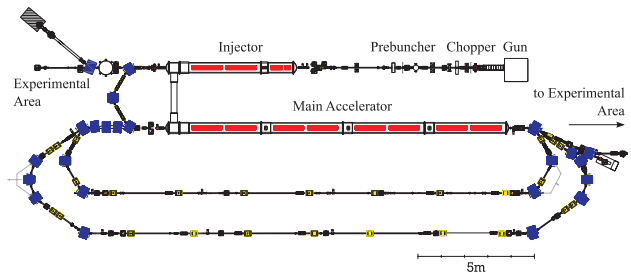

Figure 1: Floor plan of the S-DALINAC.

CONTROL LOOP

In order to control the amplitude and phase of the sc cavities a Self Excited Loop (SEL) [2, 3], which is simplified shown in Fig. 2, is used inside the existing control system. The control loop measures the phase and the amplitude with two different detectors. After subtraction of the set points and the amplification of the error signals the new control signals for the phase and amplitude controllers are generated. The amplitude modulation of the existing control system consists of a simple proportional controller. Due to the fact that I/Q domain is used to process the phase inside the existing control system a Complex Phasor Modulator (CPM) [4], which decouples the amplitude and phase characteristics of the loop, is used to control the phase. The CPM controls the phase by adding a small orthogonal vector to the loop vector. The loop phase is set by the phase shifter, which is needed for the start conditions of the SEL. If the loop phase is a multiple of 2π and the loop gain is greater than 1, the SEL starts to oscillate from noise even when the resonator and the generator have different frequencies. This is an important reason for handling sc cavities with a

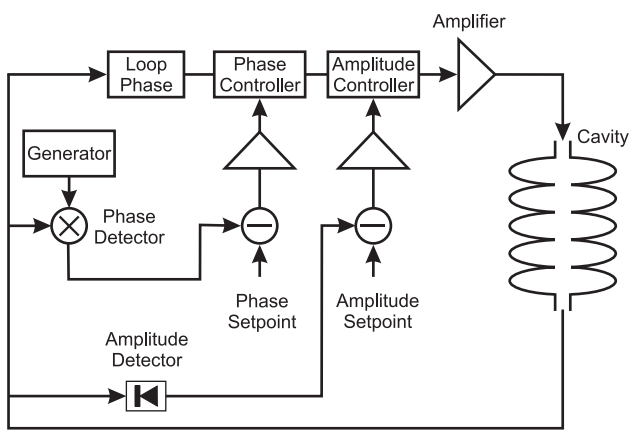

Figure 2: Self Excited Loop diagram.

loaded quality of $3 \cdot 10^7$ and a resonance width of some 100 Hz. Therefore also the new digital RF control system uses a SEL to control amplitude and phase of the sc cavities with a modified algorithm.

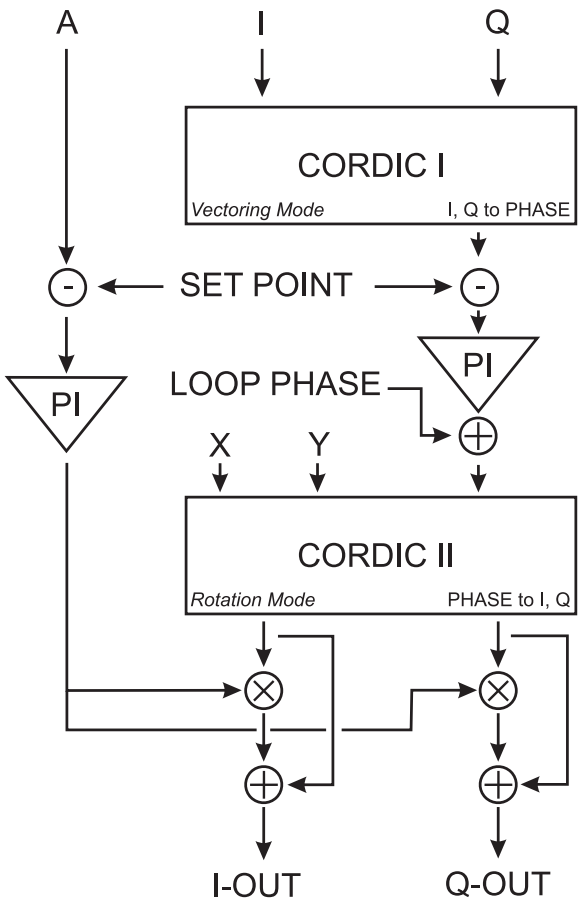

Figure 3: Diagram of the new algorithm.

CONTROL ALGORITHM

A simplified scheme of the new control algorithm is shown in Fig. 3. It starts on the top with the readout of the ADC channels for the amplitude (A) and the Cartesian phase coordinates (I and Q). The amplitude control loop uses a separated detector, which bases on our design constraints. After the subtraction of the set point a proportional and integral controller are used to process the error signal and to generate the new control signal. The phase control loop is done in a more complex way. In order to realize the phase controller like the amplitude controller with a proportional and an integral controller, the new phase modulation changes the domain from I/Q into phase. Therefore an iterative algorithm, which is called COrdinate Rotation Digital Computer (CORDIC) [5], converts the Cartesian (I/Q) to Polar (phase and amplitude) coordinates. After the phase processing the domain is changed back with a second CORDIC to I/Q again. The last step is the amplitude modulation. The amplitude control signal has a range from –1 up to 1. To avoid a mirroring of the I/Q signal created through a negative amplitude control signal, the previous I/Q signals are added on the amplitude modulated I/Q signals, which takes care that the output signal will be zero if the amplitude is to high.

The new control algorithm can be used as a SEL, if the input vectors for the first and second CORDIC are the same vectors. Furthermore it is possible to use the same algorithm as Generator Driven Resonator (GDR), if a constant vector is used as input for the second CORDIC, which is important for the operation of normal conducting copper resonators with low Q used in the low energy part of the injector of the S-DALINAC.

NEW RF CONTROL SYSTEM

Hardware

The design of the new developed RF control system follows the existing low level RF control system, making use of modern highly integrated components offering better performance. The control system consists of two main parts. The new RF-board, which consists of commercial available wifi components with excellent stability against a variation in temperature and low noise, is shown in Fig. 4. It converts the 3 GHz signals down to the base band and not to an intermediate frequency like elsewhere [6].

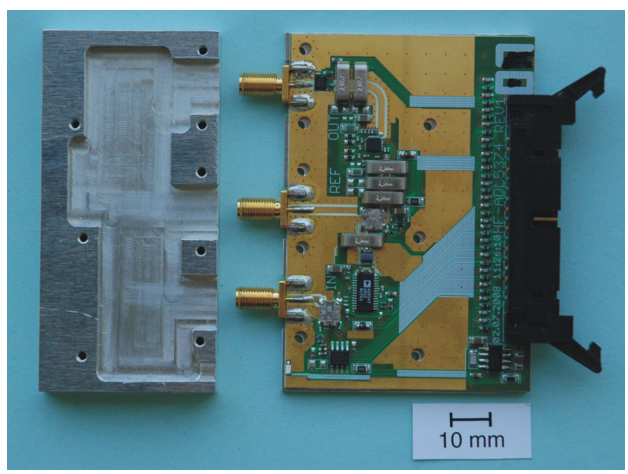

Figure 4: Picture of the new RF-board.

The analogue low frequency signals for the demodulated I/Q phase and the amplitude are transmitted to a FPGA-board. That module is shown in Fig. 5. There the analogue signals are digitized with a sampling rate of 1 M samples per second and processed inside a FPGA using the control algorithm which is presented above. After the processing of the control loop is finished the new control signals are transformed to analogue ones again and transferred back to the RF-board. The low frequency control signals are modulated on the 3 GHz RF again with an I/Q modulator.

One of the most important features of a digital solution, based on a FPGA, is the great flexibility. The same hardware can be used to realize different and more

complex control loops, which allows a better comparison of the results. These loops can be programmed into the FPGA with VERILOG. The programming of the first loop took several months until the right parameter settings and the right amplification of the error signals were found. The developed digital FPGA-board has a further advantage. The implemented USB 2.0 interface is used for an extensive diagnostic of the control loop. This interface is used to read out up to eight parameters inside the control loop in real time and a high resolution without data reduction. During the first operation a software oscilloscope was used to visualize the control loop parameters in real time. In addition it was possible to record the data. This allows an extensive data analysis, which is important for the optimization of the control parameters. A CAN bus interface was used to set the new parameters inside the control loop.

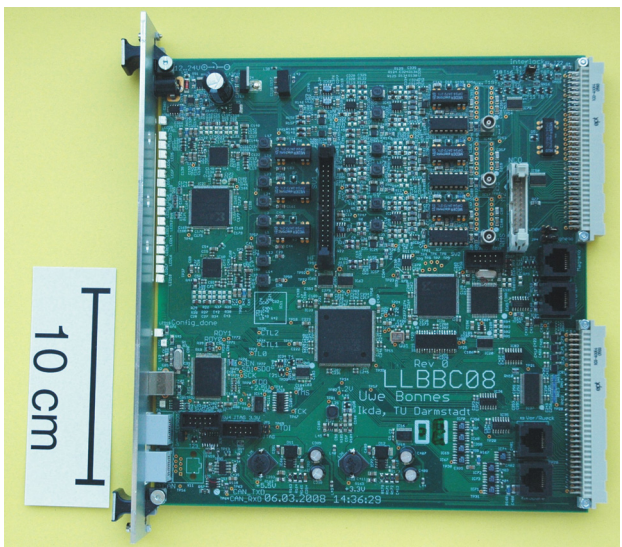

Figure 5: Picture of the FPGA-board.

Performance

The performance of the new RF control system was proved under realistic conditions. For the measurement a standard 20 cell cavity inside the injector was driven with the new system. The amplitude of cavity was set to 3 MV/m and the loaded quality factor was some of $3 \cdot 10^7$. The accelerated beam current was up to 20 µA, which is a typical operational situation. During the test the new RF control system showed, compared with the existing analogue RF control system, a convenient and easy behavior. When the new control loop locked the set points for the amplitude and the phase, there could no residual offsets be observed. The phase control loop achieved with an error magnitude of 0.3° (RMS) the recommended specification given in Table 1. Unfortunately amplitude control loop exceeds the specification with a error magnitude of $2.5 \cdot 10^{-4}$ (RMS) by a factor of approximately 3. In comparison with the existing control system the amplitude error magnitude reaches an improvement of a factor of 8. To increase the amplitude stability further improvements of the control algorithm will be necessary.

CONCLUSIONS

The new digital RF control system of the S-DALINAC has been presented. It consists of the two modules a FPGA- and a RF-board, which are connected via a plug connector. The RF-board converts the 3 GHz high frequency signals down to the base band. The low frequency signals are transferred to the FPGA-board. The signal processing is done by a fast FPGA.

During the first operation the new RF control system was able to lock the phase and the amplitude of a superconducting cavity and a beam could be accelerated. The accuracy of the new RF control system has been measured and it exceeded the analogue system. Further improvements inside the control algorithm are necessary, in order to reach the recommended amplitude stability. Nevertheless the new system is ready to replace the analogue one and the improvements of the algorithm can be done parallel to the operation of the new system.

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