DEMONSTRATION OF AN ATCA BASED RF CONTROL SYSTEM AT FLASH

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Abstract

Future rf control systems will require simultaneous data acquisition of up to 100 fast ADC channels at sampling rates of around 100 MHz and real time signal processing within a few hundred nanoseconds. At the same time the standardization of Low-Level RF systems are common objectives for all laboratories for cost reduction, performance optimization and machine reliability. Also desirable are modularity and scalability of the design as well as compatibility with accelerator instrumentation needs including the control system. All these requirements can be fulfilled with the new telecommunication standard ATCA when adopted to the domain of instrumentation. We describe the architecture and design of an ATCA based LLRF system for the European XFEL. The operation of a prototype capable of controlling the vector-sum of 24-cavities and providing measurements of forward and reflected power are presented.

CONCEPTUAL DESIGN OF LLRF BASED ON THE ATCA STANDARD

The LLRF system for each rf station at the European XFEL must support acquisition of more than 100 ADC channels and data processing of all these channels on a time scale of several hundred nanoseconds to set the actuator for the klystron drive signal for cavity field control. Fast piezotuners are used to compensate the Lorentz force detuning during the pulse. The architecture of the RF system for the European XFEL is shown in Figure 1.

Overall of the order of 100 applications will be implemented to ensure good field control, simple operation and high availability. The time scale for these applications range from some 100 nanoseconds over microseconds to milliseconds and seconds. The signal processing architecture with the communication links must be designed to support the required applications. The main requirements for the electronics standard are:

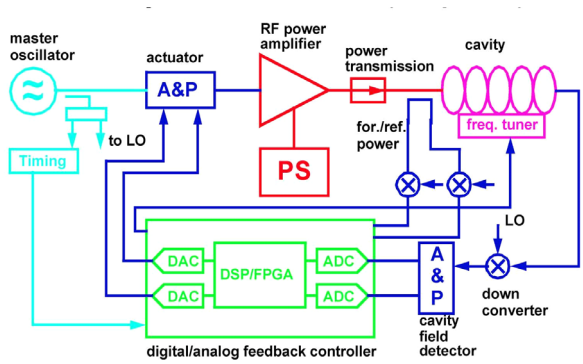

Figure 1: LLRF system architecture.

- Modularity
- Scalability
- Availability of COTS components
- Long term support
- Low latency, high bandwidth communication links
- Support signal processing in a distributed heterogeneous system of processors (FPGA, DSP, CPU)
- Compatibility with accelerator control system hardware and software.

The ATCA solution is composed of several ATCA carrier boards with 3 slots for AMC modules with different functionality. The carrier board includes a large FPGA (Virtex V) for low latency signal processing, and a DSP (TigerSHarc) for floating point operations. The following AMC modules types are required for rf control:

- 8 channel ADC
- 8 channel DAC
- Vector-modulator with 2 DACs
- Timing receiver with clock synthesizer
- 8 channel piezo-driver
- Signal processor card with FPGA and or DSP
- 8 channel optical GbE

The downconverters are be mounted as mezzanine cards on rear transition modules (RTM). This board is designed with only a few active components to improve the MTBF. All signals are connected from the rear of the shelf.

GOALS OF THE DEMONSTRATION

The various technical aspects that are verified during the demonstrations are listed in Table 1.

Table 1: Aspects of Demonstration

Objective	Comment
Analog IO	Demonstrate that noise added to the signal from the input to rear transition module through Zone 3 and carrier board to the AMC module is not degraded
Communication links	Demonstrate that the scheme of low latency links, PCIe and GbE is functional.
Operation in the accelerator environment	Demonstrate that the ATCA based LLRF is functional in the noisy accelerator environment.
Rear transition module	Demonstrate the concept of rear transition modules with downconverters.
Timing distribution	Demonstrate that the timing distribution system is functional.
Timing jitter	Demonstrate that the measured timing jitter is adequate for LLRF control.
IPMI	Demonstrate the IPMI implementation.

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In this paper we describe the last phase of the demonstration with control of 24 cavities.

HARDWARE ARCHITECTURE

The hardware used in the demonstration consists of an ATCA CPU Blade Adlink 6900, 4 ATCA carrier boards, 6 8-channel ADC AMC cards (TAMC900 from Tews), AMC cards for the vector-modulator (VM) card with DACs (in-house design), and downconverters on the rear transition module. The block diagram of the hardware is presented in Figure 2. All required signals such as the external source for the rf reference and clock and timing signals are supplied from the FLASH accelerator facility. The probe signals from the cavities and the Local Oscillator (LO) signal with a frequency of f_{LO}=1.354 GHz are connected to the downconverters. The output signal with an intermediate frequency of f_{IF}=54 MHz is connected to a data acquisition module (TAMC 900). The probe signals are sampled at a clock frequency of f_S=81 MHz during the rf pulse. The sampled data are send from the ADC card to the VM card via low latency links (LLL) with a maximum latency of 120 ns.

The LLRF controller is implemented in the Xilinx FPGA V5 on the TAMC900 module. The processed output signal is converted into analogue I and Q components and send to the input of the vector modular which drives the preamplifier of the klystron. Communication between the hardware componentes is accomplished via PCIe interface and Gigabit Ethernet.

During the demonstration at FLASH the LLRF system (shown in Figures 3,4,5) has been connected to the 24 cavities in cryomodules 4-6.

LLRF Carrier and RTM

The hardware used during the demonstration uses a combination of commercial an in-house designed boards. A block diagram with the hardware used during the demontration is presented in Figure 2. The ATCA carrier board with three AMC bays and customized analog signal routing in Zone 3 has been designed at DESY. The other components are connected or mounted directly on the carrier board. The custom designed eight channel downconverters are installed on the RTM board. LO and probe signals are connected to the RTM. The DAQ module is installed in AMC bay on the ATCA carrier board. All required signals are provided by the carrier: 8 analog signals from downconverters, low latency links to the VM and main FPGA. The VM module is installed in the second AMC bay. Low latency connections are required for the transmission of real-time data from DAQ

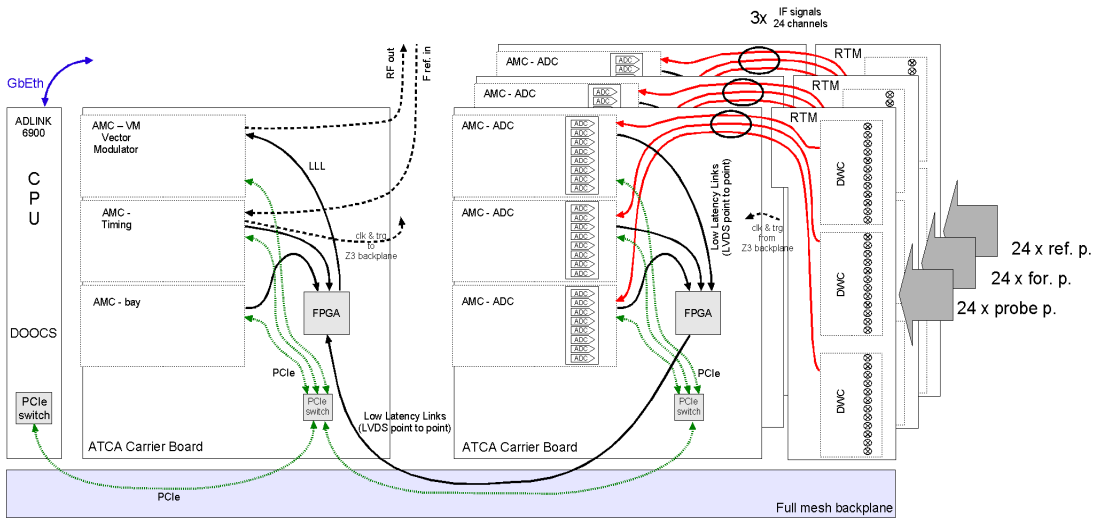

Figure 2: Hardware block diagram for the demonstration.

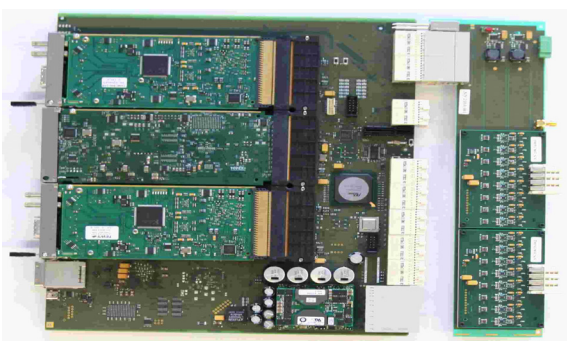

Figure 3: ATCA LLRF system consisting of ATCA carrier, AMCs and RTM module with downconverters.

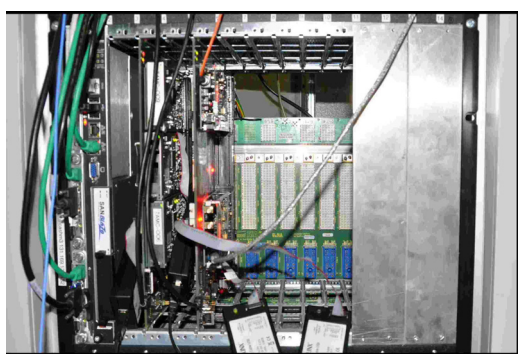

Figure 4: ATCA LLRF system.

to VM. The main LLRF controller is implemented in the FPGA present on the VM module.

The carrier board contains a PCIe switch that is connected to an external PC computer. The computer operates as a Root Complex device required by PCIe interface. The configuration parameters of the LLRF controller can be send via Gigabit Ethernet to the PC computer and forwarded to the destination device via PCIe connection.

SOFTWARE ARCHITECTURE

The software architecture prepared for the test is presented in Figure 5. The software consists of VHDL and C/C++ components. The VHDL components were implemented in FPGA chips located on carrier blades and AMCs. The C/C++ software is implemented in ATCA CPU blade located in slot 1 of the ATCA shelf.

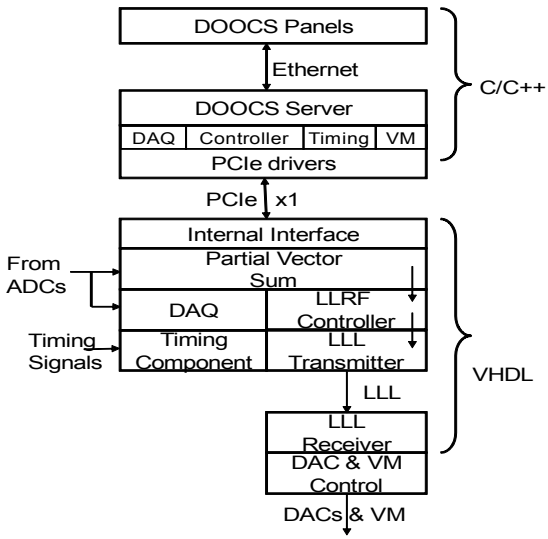

Figure 5: Architecture of software used in tests.

There are several VHDL components implemented in 15 FPGAs in the ATCA system. Some of the components are implemented in a FPGA such as the LLRF controller and DAC & VM control as well as timing components. The others like DAQ or partial vector sum are implemented in several FPGAs. The DAQ component collects data from several places in the system such as ADCs, LLRF controller and VM and makes it available to other VHDL components and to the software. In parallel the partial vector sum is calculated from ADCs data and sent to the LLRF controller. The controller generates a control signal which is sent through low latency links over the ATCA backplane to the DACs & VM Control component which drives the klystron. The Timing Component receives trigger events and clocks from the FLASH timing and synchronizes operation of the LLRF controller as well as sends interrupts through PCIe to the DOOCS server. All of the VHDL components have status and control registers represented by the Internal Interface block shown in Figure 5. Each VHDL component has an independent address space. The CPU communicates with VHDL components through PCIe links over the ATCA backplane and the PCIe switches located on every carrier blade. Each VHDL component is represented in the operating system as a PCIe device and it has its distinct entry in the PCIe tree structure. All VHDL components are controlled by a DOOCS server. The DOOCS server is modular, consists of several C++ classes representing model and functionality of each VHDL device. On the other side the DOOCS server makes high level functions of the devices available to user control panels.

The throughput of PCIe was sufficient for transmitting all DAQ data between subsequent RF pulses. All functions of the system were controlled from the DOOCS control panels.

SYSTEM PERFORMANCE

The noise level measured in the set-up in Figure 4 without rf input signals is around 200μV (rms). The result of a measurement of a cavity probe signal is shown in Figure 6. The IF frequency of 54 MHz has been sampled with a 81 MHz clock. The resulting phase jitter of about 0.25 deg. rms at the full measurement bandwidth of 200 MHz will be reduced to about 0.02 deg. rms at the closed loop bandwidth of about 20 kHz.

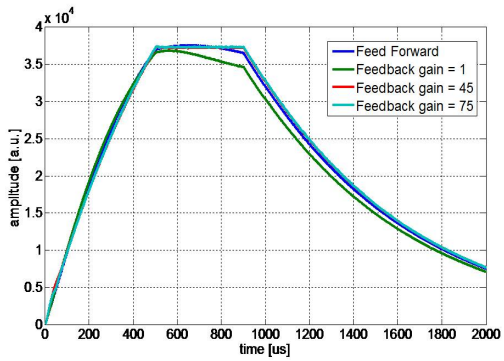

Figure 6: Amplitude control feedback gain.

SUMMARY

The initial experience with the new ATCA standard applied for instrumentation and control purposes has been very positive. The demonstration at FLASH has proven that the ATCA standard can be used for instrumentation purposes where many channels of small signal levels must be processed with low noise of and low latencies of a few hundred nanoseconds.

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