A PICO-SECOND STABLE CLOCK AND TRIGGER DISTRIBUTION SYSTEM FOR THE EUROPEAN XFEL

P. Gessler*, K. Rehlich, DESY, Hamburg, Germany
C. Bohm, A. Hidvégi, Stockholm University - Physics Dept., Stockholm, Sweden

Abstract

For the operation of the European X-Ray Free Electron Laser (XFEL), a system wide synchronous low-jitter clock and precise, adjustable triggers must be generated and distributed throughout the 3.5 km long facility. Consumers are numerous diagnostics, controls, and experiments. Fast ADCs require the jitter of a distributed 1.3GHz clock to be in the order of a few pico seconds (RMS) and synchronized to the accelerating RF. Due to cable lengths, and the temperature dependence of the propagation speed, temperature drifts are a serious issue. Therefore a complex monitoring and compensation mechanism has been developed to minimize these effects. The hardware platform of the XFEL will be based on the new standard µTCA and ATCA. Therefore the timing is implemented as an AMC (Advanced Mezzanine Card) module that fits into both crate systems. A prototype of this new clock and trigger system has been developed and first measurements have shown, that the strong requirements can be fulfilled.

INTRODUCTION

The European X-Ray Free Electron Laser (XFEL) [1] will be build over the next few years at DESY in Hamburg, Germany. With electron beam energies of 20 GeV and bunch length of 80 fs it will produce photon beams with peak powers of 135 GW and durations of 100 fs.

Defining the timing system as a clock and trigger generation and distribution system for almost all standard diagnostics, the XFEL design challenges the system in two ways: the stability of the signals and maintaining it over up to 3.5 km long fibre connections.

Most important is the stability of the delivered clocks and triggers. As they are used for diagnostic devices like analog-to-digital converters (ADC) to sample physical parameters of the electron or photon beam the clock needs to be stable relative to the accelerating RF. Additionally the triggers need to be stable relative to the bunches in the machine.

As the sampling frequencies of the ADCs increase also the sensitivity to phase jitter increases as it degrades the signal to noise ratio of the measurement. Also long term drifts have a bad influence on sampled data, as it moves the sampling points relative to the beam. Therefore the integrated timing jitter (short and long term) of the final timing system should be below 10 ps rms (for further requirements on the timing system see [2]).

* patrick.gessler@desy.de

The main problem is to maintain the stability at the sender over the up to 3.5 km long optical fibre links to the receiver cards. Due to temperature changes the fibres become effectively longer or shorter which causes phase drifts at the receiver. Therefore a complex compensation scheme was designed to reduce those drifts to a minimum.

The final timing system will distribute the timing signal in a star topology to more than 100 end points. The transmitted timing signal consists of a digital data stream which encodes the trigger events and runs with 1.3GHz (synchronous to the accelerating RF). At the receiver side the 1.3GHz reference clock and the trigger events will be recovered and used for providing different frequencies and triggers. All hardware will be based on Advanced Mezzanine Cards (AMC) for micro telecom computing architecture (MicroTCA).

In previous measurements we had already shown, that the components' short term jitter stay well below the aspired goal of 10 ps [3]. We also showed in a test setup, that the drift compensation scheme was able to reduce the drift down to 3.3 ps under high temperature changes on the fibre [4]. In this paper we will present the first developed prototype board and give an overview of its features.

HARDWARE

The major functional blocks are highlighted in Figure 1 and will be described briefly in the following paragraphs.

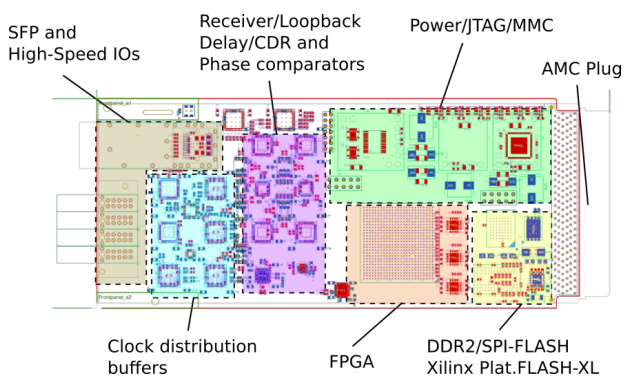

Figure 1: Functional blocks of the prototype timing AMC module.

A picture of the first developed prototype timing system module is shown in Figure 2.

It is designed as an Advanced Mezzanine Card (AMC) to be compatible with the MicroTCA and ATCA standards which will be used for XFEL.

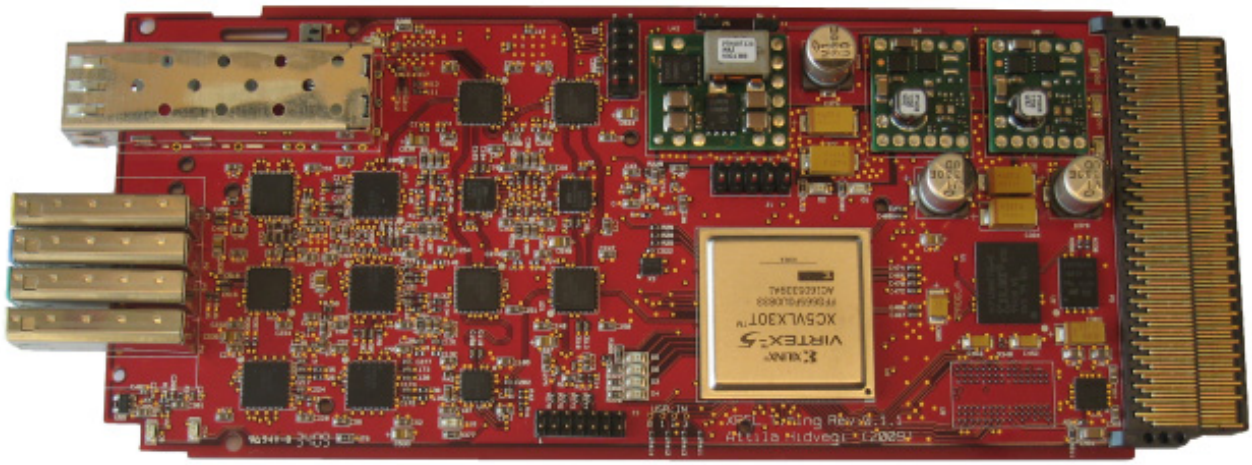

Figure 2: Prototype of the timing AMC module.

Power, JTAG and MMC

An important function of AMC modules is the ability to be managed in terms of enabling or disabling the card, monitor temperatures and power consumption, provide information about different parameters, and so on. This will be accomplished by a shelf management system and a Module Management Controller (MMC). Beside the MMC and the power supply electronics there is also a JTAG (Joint Test Action Group) interface for programming and configuring the MMC controller.

FPGA

The central element on the timing system module is a Field Programmable Gate Array (FPGA). In this case a Virtex 5 FPGA from Xilinx [5] were used.

Some of the main functions are to configure all connected chips, decode the timing signal, generate programmable triggers, patterns and low precision clocks and to re-synchronize the outputs to the reference clock.

SFP and High-Speed IOs

A Small Form-factor Pluggable (SFP) socket is build on the card to accommodate an optical transceiver. This is used for transmitting and receiving the timing signal.

Additionally there are four Har-Link [6] connectors implemented which offers different high-speed inputs and outputs for clocks, triggers and the timing signal.

Receiver and Loopback

This block implements recovering of the reference clock of the timing signal, drift compensation, timing signal generation and transmission of the timing signal. It is designed to support transmitter and also receiver mode, so that two of these cards could be used to implement a whole link of the timing system.

Clock Distribution

Besides the clock distribution this part also includes multiplexers to choose between different clocks, offers dividers and shifters and output drivers.

Memory

Two types of memories are implemented on the board. A DDR2 memory offers a high-speed data storage for the FPGA. And an FLASH memory stores the firmware for the FPGA and is loaded on power-up.

FEATURES

As mentioned before, a main design goal was, that the prototype could be used as generator and transmitter of the timing signal as well as a receiver and clock and trigger distribution unit.

The main features are as follows:

- Receive/Transmit and decode/encode timing signal
- Drift compensation (between transmitter and receiver)
- Clock cleaning
- Synchronisation of different receivers
- Deliver programmable triggers
- Deliver programmable patterns
- Deliver programmable clocks

The prototype board offers one SFP module for the optical timing signal as well as four Har-Link connectors for the following interfaces:

- Optical SFP transceiver for timing signal
- Differential input and output for timing signal
- 2 additional clock inputs (reference or local clocks)
- 6 dedicated clock outputs
- 2 clock outputs to the backplane
- 5 clock-or-trigger outputs
- Different standards: LVDS, LVPECL, LVTTL, CMOS

CONCLUSION AND OUTLOOK

The designed prototype offers all possibilities to setup and investigate the proposed timing system for XFEL.

In the next step the firmware for the FPGA needs to be further developed to support the different functions needed in order to establish the timing system. After that further measurements need to verify, whether the aspired stability could also be maintained at the different outputs over a distance of 3.5 km and what design changes need to be considered.

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[5] http://www.xilinx.com/.

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