

COMMERCIAL-OFF-THE-SHELF TECHNOLOGIES FOR PICOSECOND TIMING AND SYNCHRONIZATION

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Abstract

Accurate timing is a key aspect of large physics experiments. More and more, Commercial-Off-The-Shelf (COTS) technologies are used to provide synchronization down to a few picoseconds. This approach allows a wide selection of equipment, offers a high level of flexibility, and guarantees a smooth evolution as new technologies become available. For example, Greenfield Technology proposes a picosecond timing system that provides several hundred triggers to equipments distributed over an area of thousands of square meters within a resolution of 1 ps and low jitter < 15 ps. This system is built around a central oscillator transmitter which delivers a serial data stream over an optical network to manage delay generator triggering and time base. By combining this distributed timing system with the clock and triggering synchronization features of the PXI backplane, high speed instruments, such as digitizers, can also be synchronized with picoseconds accuracy to guarantee the best measurement quality.

INTRODUCTION

A typical distributed timing system requires the following components:

- **A master source**, able to respond to an external trigger or generate an internal trigger. In some cases the master source can also generate a shared clock for the entire system.
- **A network**, responsible for distributing the trigger, and the clock if it exists, to the various sub-systems. This network will typically use optical fibers for distribution over a large area, or electrical cables for smaller areas.
- **Several delay generators**, which can be programmed with very fine delays (typically well below 1 ns) to precisely control the triggering of various instruments and sub-systems.

The performance of such a system is usually measured by the jitter between triggers, the delay resolution and accuracy, as well as the drift, or stability, over long periods of time. Other factors such as maximum delay, flexible triggering modes, control of the trigger amplitude and pulse width, ease of programming, form factor, or cabling complexity should also be considered.

Ultimately the performance of any timing system has to be matched by the instrumentation it is driving, so that the overall system performance meets the requirements of the experiment. Typical applications include, among others, high power lasers, synchrotrons, ion beams, and inertial fusion targets.

TIMING SYSTEMS

Greenfield Technology offers various products that can be used to successfully meet the requirements of even the most demanding distributed timing system. Two typical architectures are presented below, one using optical fibers for the network, the other one using electrical cables.

Optical Network

The overall system architecture is shown in Fig. 1. The GFT3001 clock transmitter allows the distribution of a synchronous master clock over the entire system. The GFT3001 can be triggered by an external signal or can generate its own internal trigger(s). For synchrotron applications, up to 255 delayed triggers can be defined, as single shot or repetitive, and as part of a single or multiple sequences. On the other hand, for laser applications, up to 3 independent repetition rates are possible, from 0.1 Hz to 1 kHz. All sub-frequencies are exact divider of the master clock and are distributed over the entire system.

The optical network allows the distribution of the proper signals to all delay generators.

The GFT1404 (in development) or GFT1218 digital delay generators receive the optical signals from the transmitter, decode them, and then generate the local trigger signals. As all delay generators are using the same clock, the jitter for long delay is essentially the same as the jitter of the master clock.

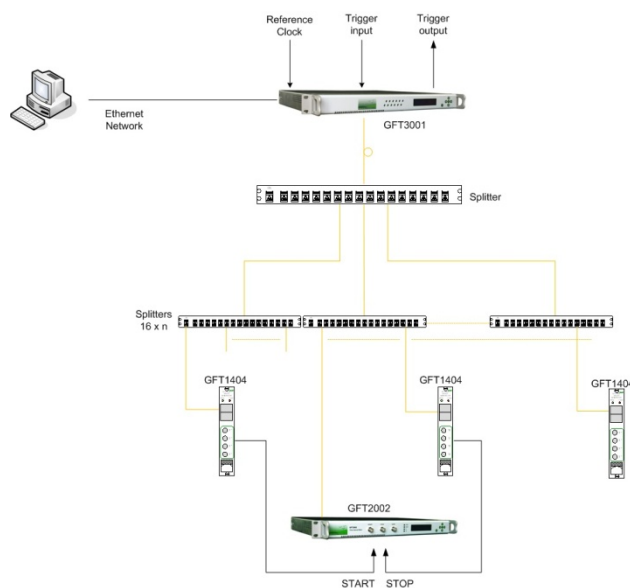


Figure 1: Timing system using optical network.

Electrical Network

In this configuration the basic architecture relies on the distribution of a single master trigger to numerous sub-systems using digital splitters such as the GFT4208. By daisy chaining several splitters it is possible to deploy configurations of up to 1024 triggers.

This architecture can be extended to include the distribution of a master reference clock to the entire system. A clock frequency of 10 MHz is typically chosen as it can be used for synchronization, not only of the timing system, but also of most instruments. Applying this concept to the PXI platform is now straightforward by combining the National Instruments (NI) PXI-6653 timing and synchronization board and the new GFT9404 PXI delay generator. An example of such a configuration is presented in Fig. 2. This configuration takes advantage of the timing and synchronization capabilities of the PXI platform as detailed below.

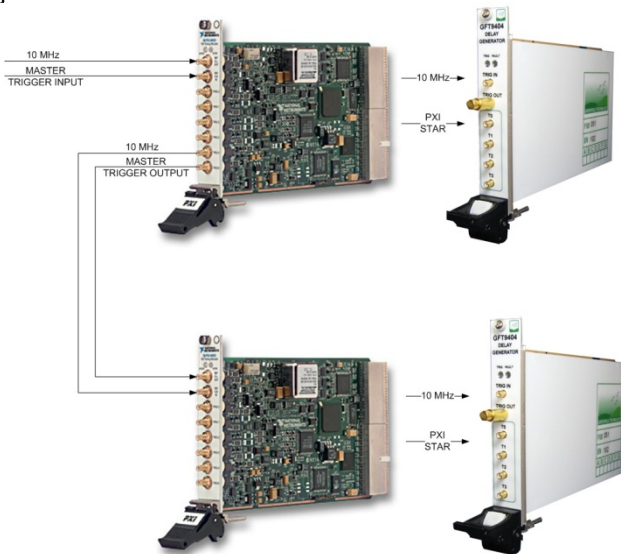


Figure 2: Timing system using electrical network and shared 10 MHz clock.

Table 1: Timing System Performance

	Optical	Electrical	Electrical + Clock
Maximum distance	1000 m	10 m	50 m
Trigger source	External or internal	External	External or internal
EMI immunity	Better	Good	Good
Clock frequency	100 to 200 MHz	N/A	10 MHz
Jitter – Master trigger input to output delay	One clock period	< 50 ps rms	< 100 ps rms
Jitter – Master trigger output to output delay	< 30 ps rms	< 50 ps rms	< 50 ps rms

Performance

Table 1 presents a summary of the typical performance measured for the different configurations described in this article. We used a GFT2002 time interval meter for the delay and jitter measurements (see Fig. 1).

PXI PLATFORM

Overview

PXI (PCI eXtensions for Instrumentation) is a rugged PC-based platform. PXI combines the PCI data bus with the rugged, modular, Eurocard packaging of CompactPCI, and then adds specialized synchronization buses and key software features to satisfy requirements for deterministic timing and triggering.

PXI is an open industry standard, offering more than 1,500 products from the 70+ members of the PXI Systems Alliance. PXI also preserves investments in stand-alone instruments, VME, and VXI (VME eXtensions for Instrumentation) systems by providing standard hardware and software for communication to these systems. This provides the flexibility to build hybrid systems interfacing instrumentation across any bus.

Timing and Synchronization in PXI

One of PXI's main advantages is its ability to tightly synchronize its many I/O channels. The timing and synchronization architecture for PXI evolved from that used in the VXI architecture. VXI provided 8 TTL trigger lines and 6 ECL lines that could be driven and received from any module. The PXI_TRIG bus described below follows this architecture. In addition to this trigger bus, PXI has added three additional timing and triggering features to improve the level of synchronization between modules (see Fig. 3):

- PXI_CLK10 provides a 10MHz clock to each slot in a PXI chassis. This clock is matched in skew to < 1ns slot-to-slot and can be used to provide a common clock domain to all modules in the system.
- PXI_TRIG is an 8-line parallel trigger bus that provides general purpose triggers between slots.
- PXI_STAR provides point-to-point, matched-skew (< 1ns slot-to-slot) to each module from the system timing slot (slot 2 in PXI).

All of these timing and triggering features are accessible via the system timing slot. This particular slot allows the user to import/export the clock and to distribute the external trigger to the other slots via the Star trigger bus. This also allows the distribution of a common clock to several PXI chassis, ensuring that every PXI delay generator and instrument uses the same clock reference. Various delays can be generated by the GFT9404 board and distributed to the instruments via their front panels or the PXI trigger bus.

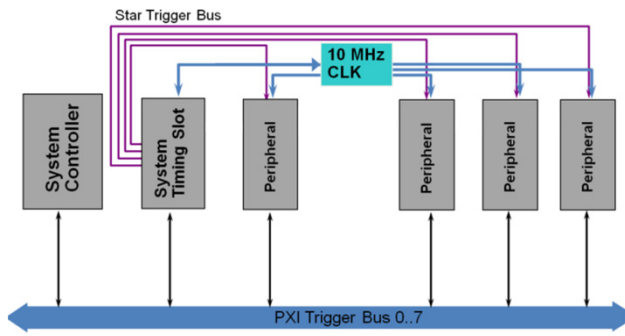


Figure 3: PXI timing and synchronization architecture.

Synchronization Challenges

Distributing clocks and triggers to achieve high-speed synchronized measurements is beset by nontrivial issues. Latencies and timing uncertainties involved in orchestrating multiple-measurement devices are significant challenges in synchronization, especially for high-speed measurement systems. Two main issues that arise in the distribution of clocks and triggers are skew and jitter.

The instrumentation of large physics experiments often requires different sampling rates on each instrument. But they need to be synchronized, and more importantly, data needs to be sampled on the correct sample clock edge on each instrument. When sample clocks on disparate instruments are integer multiples of the 10 MHz reference clock, all instruments will have sample clocks that are synchronous to each other – the rising edge of all sample clocks will be coincident with the 10 MHz clock edge. When sample clocks are not integer multiples, such as 25 MHz, there is no guarantee that the sample clocks are in phase, despite being phase-locked to the 10 MHz reference clock. Standard techniques are used to solve this problem by resetting all of the phase-locked loops (PLLs) at the same time, leading to sample clocks of the same frequency being in phase. Even though all sample clocks are in phase at this point, the solution is still not complete. Perfect synchronization implies the data clocked from device to device corresponding to within a sample clock cycle. The key to perfect synchronization is triggering.

With sample clock synchronization addressed, the other main issue is the distribution of the trigger to initiate simultaneous operation. Two issues that arise here are trigger delay and skew. A trigger delay from the master to all the slaves and skew between each slave device is inevitable, but this delay and skew can be measured and calibrated. The challenge in measuring the delay and skew, however, is a two-part process:

- Automate the measurement of the trigger delay between master and each slave and compensate for it.
- Ensure that the skew between slaves is small enough to guarantee that the trigger is seen on the same clock edge on all devices.

The distribution of the trigger signal across multiple devices requires passing a trigger signal into the clock

domain of the sample clock such that the trigger is seen at the right instance in time on each device.

With sample clock rates higher than or equal to 100 MS/s, skew becomes a major obstacle to accurate trigger distribution. A system consisting of several 200 MS/s digitizers, for example, requires a trigger being received at each device within a 5 ns window. The trigger signals must be sent in a slower clock domain than that of sample clock and transferred to the high-speed sample clock domain. A logical choice is to synchronize the trigger signal distribution with the 10 MHz reference clock. However, this cannot ensure that two boards will see the trigger assertion in the same sample clock cycle when the sample clocks are not integer multiples of the 10 MHz reference clock.

Synchronization with Trigger Clock

The purpose of TClk (Trigger Clock) synchronization is to have devices respond to triggers at the same time. The "same time" means on the same sample period and having very tight alignment of the sample clocks. TClk synchronization is accomplished by having each device generate a trigger clock that is derived from the sample clock. Triggers are synchronized to a TClk pulse. A device that receives a trigger from an external source or generates it internally will send the signal to all devices, including itself, on a falling edge of TClk. All devices react to the trigger on the following rising edge of TClk. The TClk frequency is much lower than the sample clock to accommodate propagation delays of several nanoseconds.

Robust synchronization of multiple devices can be achieved by simply inserting the devices into the PXI chassis and running the devices using NI-TClk software.

TClk synchronization can deliver synchronized devices with skews better than 1 ns between each device. The typical skews observed range from 200 to 500 ps. Still this skew may not be satisfactory for some applications where a higher level of performance is required. In this case, manual calibration is required. Manual calibration can lower skews to less than 30 ps between devices. Manual calibration involves the adjustment of the sample clock on each device with respect to each other using the phase adjustment DACs (Digital-to-Analog Converters) in the PLL circuitry. The sample clock adjustment resolution is 5 ps and can be adjusted to ± 1 sample clock period. Thus, the skew between devices can be manually calibrated with high accuracy.

CONCLUSION

By leveraging COTS technologies such as PXI it is now possible to develop complex instrumentation systems that rely on a very accurate distribution of timing and triggering signals. COTS products typically offer a high level of software integration that substantially reduces development time, and guarantee the long term evolution of software and hardware investments.