DESIGN OF A DIGITAL CONTROLLER FOR ALPI 80 MHZ RESONATORS

S. Barabin, Institute of Theoretical and Experimental Physics, Moscow, Russia
G. Bassato, INFN, Laboratori Nazionali di Legnaro, Legnaro (Padova), Italy

Abstract

We discuss the design of a resonator controller based mainly on digital technology. The signal frequency is 80 MHz but can be easily increased up to 350MHz; the controller can work in either "Generator Driven" (GDR) or "Self-Excited Loop" (SEL) modes. The signal processing unit is a commercial board (Bittware T2-Pci) with Xilinx Virtex II-Pro FPGA and 4 TigerSharc DSPs. The front-end board includes a set of A/D channels, which sample the RF signals coming from the cavity pickup and from the reference generator. We present results of some preliminary tests on 80 MHz quarter wave resonator installed in the ALPI Linac accelerator at INFN-LNL and discuss possible developments of this project.

INTRODUCTION

Low level RF control is nowadays implemented using digital techniques [1, 2]. The availability of high-density FPGAs commercial boards makes possible to implement in hardware computational functions that, in the past, would have required an array of high performance DSPs. The board we chose for our application contains both, but most of RF processing blocks (i.e. signal conversion and digital signal processing) are configured inside the FPGA, while DSPs and their memory are mainly used for data routing and several diagnostic calculations.

The general concepts and ideal characteristics of a digital controller are described in [2]. The main features currently realized in our RF controller can be summarized as follows:

- Capability of working in both SEL and GDR modes and switching between them;
- Capability of operating with both superconducting and room temperature cavities;
- Selection between I/Q and amplitude/phase control;
- Frequency sweep mode and frequency response plot generation;
- Provision for cavity frequency resonance control by means of mechanical tuner;
- Minimal use of analog components – no analog downconverters, vector modulators and phase shifters.

RF CONTROLLER DESCRIPTION

As shown in fig. 1 and fig. 2, the controller is based on three boards: the analog front-end for RF signal acquisition, the Bittware T2-PCI board [3] containing DSPs and FPGA, and an output board to generate the signal driving the power amplifier.

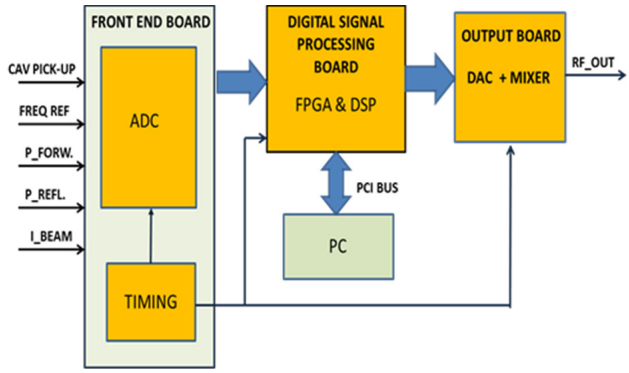

Figure 1: Resonator controller block diagram.

The analog front-end includes five A/D channels based on the AD9433 ADC. Two A/D sample RF signals coming from the cavity pickup and from the frequency reference generator. Additional ADC channels acquire information of amplifier's direct and reflected power and beam current, in order to extend the controller capability to accelerators with high current and beam loading effects. For each channel, an Epcos B39805 bandpass filter followed by a Mini-Circuits ERA-3 amplifier and an ADT1–1WT transformer provide the required filtering and impedance adaptation for the ADC input.

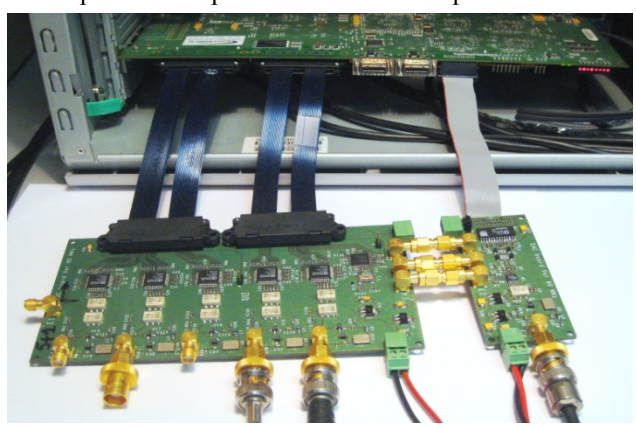

Figure 2: The controller boards.

The output signal driving the power amplifier is generated by a DAC (AD9752) at a frequency of 16MHz; after proper filtering this signal is then upconverted to 80 MHz by mixing with the 64 MHz local oscillator signal. Clock signals to 5 ADCs, DAC, mixer and FPGA are provided by the AD9516 programmable clock distributor, placed in the ADC board and featuring a channel-to-channel skew lower than 10ps. The frequency of sampling clock is 64MHz. The ADC and DAC boards are connected to the T2-PCI card through dedicated high

speed I/O channels, supporting parallel data transfer from all five 12-bit ADC and the 12-bit DAC at 64 MHz rate.

Signal Flow

Figure 3 shows the FPGA block diagram. I/Q demodulation is performed by sampling the input signals from ADCs at a frequency of 4/5 of reference signal to get a 90 deg. phase advance between two samples; the sampled I, Q components can be rotated by a rotation matrix in order to compensate the delay introduced by cables.

Digital downconversion and filtering are performed by cascaded integrator-comb (CIC) filters, to reduce signal noise. Then, signals are converted to polar form by the COordinate Rotation DIgital Computer (CORDIC) to allow phase and magnitude comparison with predefined values. The result of comparison (phase and amplitude errors) goes through a PID algorithm to generate correction signals; a further rotation on phase angle can be optionally added to compensate offsets.

Correction signals, in polar form, undergo a second CORDIC block to convert back to the complex amplitude. form. Resulting I and Q signals drive a digital quadrature modulator [4] that generates, at 16 MHz rate, patterns of 12 bit values representing samples of output signal in the time domain; these values are then sent to the output DAC.

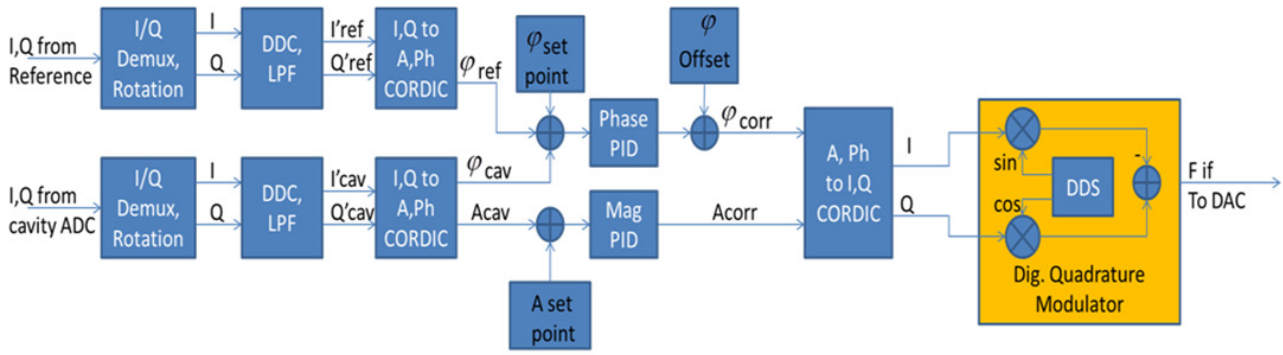

Figure 3: Signal flow inside the FPGA.

DESIGN TOOLS

The DSP code was generated by the C compiler included in Analog Devices VisualDSP++, while the FPGA project was compiled using Xilinx ISE Design Suite. Many FPGA functions are part of Xilinx System Generator module, which is a plug-in extension of Platform Studio SDK. This toolkit also supports the compilation of the PowerPC block, available in the VIRTEX-II Pro chip, we used to configure the clock generator. Matlab and Simulink (by Mathworks) were extensively used in conjunction with Xilinx System Generator module to compile and simulate several FPGA blocks.

USER INTERFACE

The program named "RF controller" implements the user interface to set and diagnose the RF field in cavity. The graphic application is written in C++ with Microsoft Visual Studio IDE. It uses Bittware's host interface library to communicate with Bittware's digital board through PCI.

User Interface Main Functions:

- Setting up desired output signal amplitude and phase;
- Switching on/off the amplitude and phase feedback;
- Select feedback type between I/Q and amplitude/phase;
- Tuning of feedback parameters like proportional and integral coefficients;
- Switching between SEL and GDR modes;
- Detection of the cavity's resonance frequency during start up (with SEL or amplitude-frequency plot);
- Tune trade-off between loop delay and noise of signal measurement, by tuning digital filters.

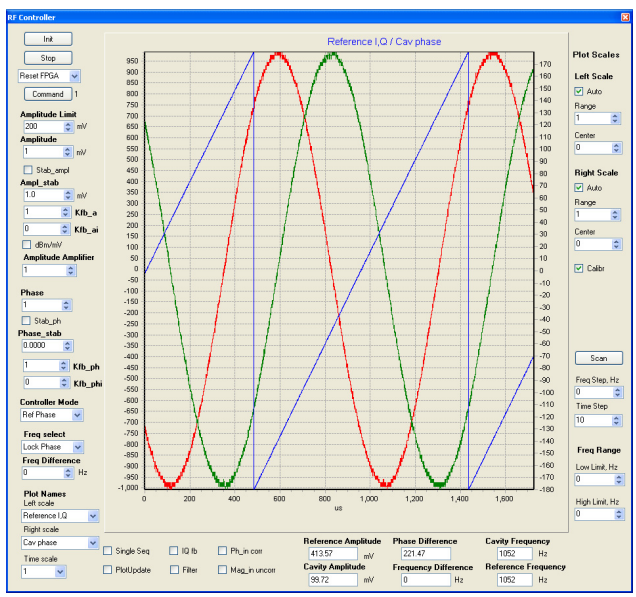

Figure 4: The "RF Controller" graphic interface.

Diagnostic Possibilities

A plot window can simultaneously present two graphs taken from different stages of signal flow. Graphs can be updated at a fixed rate, or triggered by a defined event (i.e. to view a step response). In addition, plot can show cavity's frequency response. Text windows below the plot show several parameters such as reference and cavity field amplitude, frequency and phase difference. These data are updated at approximately 8 Hz rate. Phase and frequency difference are sent by Ethernet to cavity tuner.

TEST RESULTS

Feedback Tests

Feedback capability was tested separately for amplitude and phase. Amplitude and phase PID gains have been tuned to find the optimal gain to minimize the transient response time without overshoot.

Currently, phase difference in the feedback mode can be changed with ~0.09° step, and phase difference textbox shows the same measurement value with 0.01° resolution. The signal amplitude in feedback mode can be changed with 0.1 mV (or ~0.05% from maximum value) step and measured with approximately the same resolution.

Frequency Response Tests

"RF Controller" program allows switching of the output signal frequency to the reference frequency, to the value of 5/4 of clock frequency and to any other desirable frequency (with 1 Hz step). Frequency response is achieved by automatic scan of output signal frequency.

Finding the Cavity Resonance Frequency

One possibility to find the resonance frequency on switch up is sweeping the output frequency and acquiring the cavity's response. It was shown that the reference frequency in test cavity was ~79.7 MHz, and halfwidth bandwidth was ~80 kHz.

Another possibility is using SEL mode. Before SEL mode switch-on difference between cavity and output frequency was about 300 kHz. After SEL mode activation, cavity was tuned to its resonance frequency, as visible on scope and on PC program. We also observed, after modifying cavity's resonance frequency by moving copper rings inside it, the controller was able to track frequency changes.

Feedback Tests with Cavity

It was shown that frequency locking in SEL mode is possible. Phase error in the SEL phase feedback mode was large, about 10 degrees, because of large bandwidth of the warm cavity. It is expected that the phase error for superconducting cavity can be much lower. After switching to the GDR mode (typical working mode), the phase error is reduced to 1%.

Figure 5a and 5b show the phase error under environmental disturbance conditions (mechanical vibrations) without feedback (5a) and with the cavity locked (5b) when the cavity works in generator-driven mode. The amplitude error with feedback is about 1 mV.

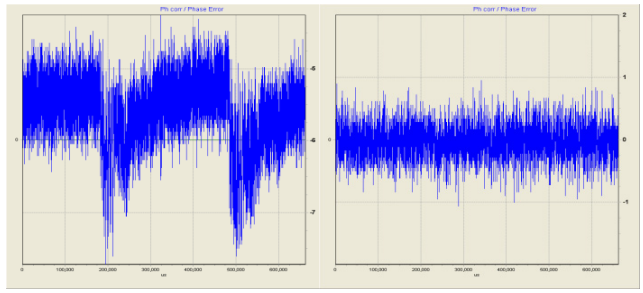

Figure 5a: cavity unlocked. Figure 5b: phase locked.

Digital Filters Addition

Amplitude and phase errors can be reduced by addition of digital filters. Using filters decreases the phase error from 1° down to ~0.25° by cost of increasing the loop delay: the loop delay, in fact, increases from ~5 to 60 µs, and the step response time grows up to 400 µs. For superconducting cavities with typical filling times up to 1 second, this loop delay is more than acceptable.

CONCLUSION

The prototype we realized demonstrates the feasibility of a digital solution fully based on FPGA. Although the preliminary results are promising, some work still need to be carried out. New features can be added by software modifications, such as:

- Feedforward beam loading;
- Power amplifier linearization;
- Any combination of amplitude, phase and I, Q control;
- Dynamic change of digital filter characteristics;
- Additional feedforward modes can be added – open loop operation at start-up, cavity conditioning/tuning, adaptive feedforward.

A significant part of hardware changes should be made by redesigning the analog section of controller, that includes: field calibration of cavity input, increase of input dynamic range by addition of variable gain amplifiers, increase of ADC resolution from 12 to 16 bit, increase of DAC resolution to 16 bit, other than its output level. Another possible change concerns with the digital board: a more modular design (i.e, changing the interface to the host computer from PCI to Ethernet) would reduce the cost, increase the flexibility and improve the performance.

REFERENCES

[1] C.Hovater et al. "A digital self excited loop for accelerating cavity field control", PAC'07.
[2] S.Simrock. "Universal Controller for digital RF Control", EPAC'06.
[3] www.bittware.com
[4] K. Gentile: "DDS simplifies polar modulation", EDN, August 2004, p69