OPEN HARDWARE FOR CERN'S ACCELERATOR CONTROL SYSTEMS

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Abstract

The accelerator control systems at CERN will be renovated and many electronics modules will be redesigned as the modules they will replace cannot be bought anymore or use obsolete components. The modules used in the control systems are diverse: analog and digital I/O, level converters and repeaters, serial links and timing modules. Overall around 120 modules are supported that are used in systems such as beam instrumentation, cryogenics and power converters. Only a small percentage of the currently used modules are commercially available, while most of them had been specifically designed at CERN.

The new developments are based on VITA and PCI-SIG standards such as FMC (FPGA Mezzanine Card), PCI Express and VME64x using transition modules. As system-on-chip interconnect, the public domain Wishbone specification is used.

For the renovation, it is considered imperative to have for each board access to the full hardware design and its firmware so that problems could quickly be resolved by CERN engineers or its collaborators.

To attract other partners, that are not necessarily part of the existing networks of particle physics, the new projects are developed in a fully 'Open' fashion. This allows for strong collaborations that will result in better and reusable designs.

Within this Open Hardware project new ways of working with industry are being tested with the aim to prove that there is no contradiction between commercial off-the-shelf products and openness and that industry can be involved at all stages, from design to production and support.

OVERVIEW OF CONTROLS HARDWARE

The Controls Group of the Beams Department (BE-CO) at CERN is responsible for the specification, design, procurement, integration, installation, commissioning and operation of the controls infrastructure for all CERN accelerators, their transfer lines and the experimental areas. The group provides services like general machine and beam synchronous timing generation and distribution (see Figure 1) and signal observation systems, as well as support for drivers and higher-level software.

As basis the group uses a set of standardized hardware and software controls components. The hardware used in the control systems is diverse: analog and digital I/O, level converters and repeaters, serial links and a range of timing modules. Overall around 120 modules are supported that are used in systems such as beam instrumentation, cryogenics and power converters.

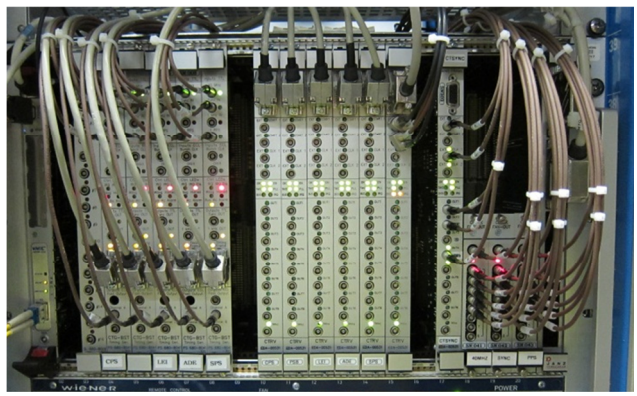

Figure 1: Timing crate controlling LHC.

Only one in four of the currently used module types are commercially available, while the others have been purposely designed at CERN. Furthermore, one in four of the module types are considered obsolete, meaning that existing modules can be maintained, but they cannot be used for new installations. These modules may have been designed up to twenty years ago and are still stocked in limited quantities. In most cases they can be repaired, but cannot be ordered or be re-produced in-house as the electronics components are no longer available.

STANDARDS FOR NEW DESIGNS

To replace the obsolete modules and to progress with new control and timing technologies, there is a continuous flow of new designs to be made.

To ease maintenance it has been decided in 2009 to base new designs on two platforms: VME64x [1] and PICMG 1.3 [2]. The latter defines an industrial type of PC that uses the PCI Express bus for its plug-in cards.

Most of the functionality that is required by the equipment groups is needed for both platforms and therefore every new device, such as a Time-to-Digital Converter (TDC) or an Analog-to-Digital Converter (ADC), would need to be designed twice. Potentially for *n* bus types and *m* functions required, *n* times *m* designs are needed.

If it were possible to put the specific required functionality on a mezzanine card, then with a single design of a carrier card for each platform, the number of designs would be reduced to n + m. The carrier card will contain basic functionality that is needed for every design,

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such as the bus interface, an FPGA, memory and other support functions while the mezzanine would only contain the specific functionality required.

Fortunately in 2009, the FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1 [3] was just published by the same organization that is responsible for the VME specifications. This standard defines a mezzanine card of around 84 mm by 69 mm in size and uses one of two connector types that have either 160 or 400 pins. There is no protocol defined for the signals on the connector as they should connect directly to an FPGA on the carrier board. As an example, Figure 2 shows such a carrier board for FMC mezzanines and uses a Xilinx Spartan 6 as FPGA. The mezzanine cards are supposed to contain only I/O logic such as buffers or an ADC, while a small front-panel space is available for external connectivity.

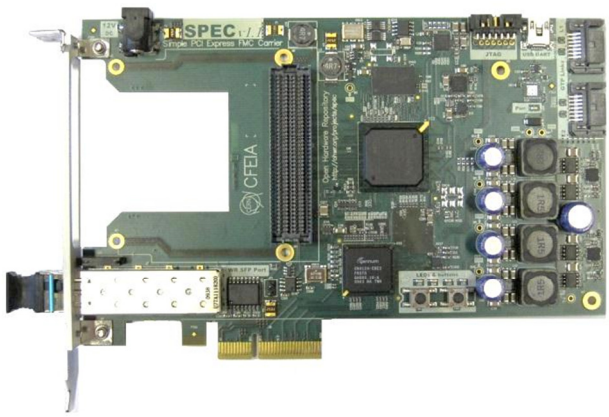

Figure 2: PCI Express carrier for FMC mezzanines developed as Open Hardware.

As many mezzanines and carriers use the same functions, the logic blocks inside the FPGA should be re-usable. To interconnect these blocks we decided to standardize on an internal bus called Wishbone [4]. Wishbone is a simple address/data bus meant to be used for system-on-chip designs and is an open standard. We collaborated in the update of the Wishbone B4 Specification to include a pipelined mode that enhances communication with high-latency high-throughput devices, such as DDR RAM controllers. Many ready-made building blocks are already available, such as Wishbone to I2C or to one-wire bus protocols.

Of course not all new designs for the control system use the FMC standard. E.g. level converters needing a large front-panel space for connectors are designed in the VME64x format.

NEED FOR OPEN HARDWARE

When new hardware is needed, in a few cases it could be bought directly from industry. This would be a resource gain as it is designed, built and tested already. At the same time it likely has proven its worth by many users in different applications. However, ready-made modules don't always have the exact functions we need. E.g., even for simple ADC modules CERN needs specific trigger modes or input capabilities that are not usual. Furthermore, when a bug is found, it may be hard to get a correction from the company as CERN's applications are very complex and the reported bugs may be difficult to reproduce. Ultimately, as there is normally no access to design documentation, it is impossible to help in solving problems.

It would be valuable if the advantages of both commercial and custom hardware could be combined. We believe we have found a way to do this by using the concept of "Open Hardware", similar to the concept of "Open Software" that has proven its worth.

The main ideas behind the Open Hardware paradigm are:

- All specifications and design files are published to benefit from peer review and to enable remote collaboration.
- All detailed production files for the hardware, including PCB production files, precise bill-of-material and assembly instructions are published so that anyone can reproduce the hardware.
- Peer reviews are actively sought for to improve the designs and make them better re-usable.

OPEN HARDWARE REPOSITORY

To allow sharing of design information, a simple web site or mailing list is not enough. Therefore, in 2008 a custom development of a collaborative tool was made and the first Open Hardware Repository (OHR) site went public in February 2009. One year later, the site was moved to the Open Source program called Redmine while in February 2011 the data was moved to a 'fork' of Redmine called ChiliProject [6]. The OHR website ohwr.org [7] now contains for each project modules such as a Wiki, a file repository, a news page and notably an issues list to keep track of found problems and required changes (see Figure 3). It is truly open as anyone can access all information.

One thing is to have the final design information available; another thing is to understand the reasoning behind certain design choices. Actually we try to have this information in the form of dedicated documents and by keeping an archive of the mail exchanges between the collaborating engineers.

At the end of August 2011, the OHR site hosted 45 active projects of which 37 are initiated by different CERN groups, while 8 are from other institutes or companies. On average each project mentions 3.6 persons as developer. About thirty projects describe hardware designs, often with associated software. Another twenty projects document re-usable IP core designs that will speed up many hardware projects. Also general software tools such as a production test environment and utilities to test the performance of ADCs are hosted.

On the OHR site there are around twenty projects related to FMC developments. E.g., one can find the complete designs of carrier boards in VME64x and PCIe format. As FMC mezzanines one can find projects of

Figure 3: Open Hardware repository project page of the Simple PCI Express FMC carrier.

ADCs using different sampling speeds (100 kSPS, 100 MSPS) and TDC and Fine delay modules with a resolution of 1 ns or better. These projects are initiated by CERN while a reconfigurable hardware interface for computing and radio (RHINO) is initiated by the University of Cape Town in South Africa. Bristol University in the UK started a Trigger/Timing Logic Unit in FMC format for use in a beam-telescope.

Examples of designs that do not use FMC are a small footprint single board ARM-based computer running Linux and a TTL to NIM level converter board in VME format. Also full designs of a network switch for the White Rabbit timing network can be found.

As many projects can re-use much of the functionality that is implemented inside the FPGAs, there is also a wide range of so-called IP-cores many of which interface to the Wishbone bus: examples are a DDR3 controller, Gennum GN4124 core, VME64x core, Wishbone serialiser and Wishbone slave register generator. Also an LM32 RISC processor core and a TDC that can be implemented inside an FPGA are fully documented in the OHR.

To the users the advantages of using the OHR are clear: not only does the collaboration tool allow one to easily work with known colleagues, but it also allows to find in a single place similar designs, examples of well documented projects and of course other engineers that have the same attitude of sharing and helping.

CERN OPEN HARDWARE LICENCE

Even for Open Hardware it is necessary to have a licence that defines the conditions under which a licensee will be able to use or modify the licenced material. Although many licences exist for developing Open Software (GNU, GPL, etc.), it appeared that there was none usable to cover hardware developments. For this reason the Knowledge Transfer Group developed the CERN Open Hardware Licence (CERN OHL) [8] that is compliant with the Open Source Hardware (OSHW) definition criteria [9]. In the spirit of knowledge sharing and dissemination, the CERN OHL governs the use, copying, modification and distribution of hardware design documentation, and the manufacture and distribution of products.

It shares the same principles as open-source software: anyone should be able to see the source (the design documentation in case of hardware), study it, modify it and share it. In addition, if modifications are made and distributed, it must be under the same licence conditions – this is the 'persistent' nature of the licence – which ensure that the whole community will continue benefiting from improvements, in the sense that everyone will in turn be able to make modifications to these improvements.

Although the CERN Open Hardware Licence was originally written for CERN designs hosted in the Open Hardware Repository, it is also used by other designers wishing to share design information.

EXPERIENCE WITH INDUSTRY

It was expected that the Open Hardware paradigm would change the model of how to work with industry. When commercial hardware was needed for CERN's accelerator control systems, it was usually obtained from companies with thirty or more staff. Now as the design information is open, there is no risk that a design will be unmaintainable when a company closes or an engineer leaves. This allows CERN to work with companies that are often much smaller in size. In the past two years, to speed up the development of specialised hardware and notably for the development of firmware of interfaces to Wishbone or VME64x, we have used the services of over twelve companies in eight different countries.

We have also seen that a large company is interested in developing hardware based on the White Rabbit timing protocol specification for which several Open Hardware projects are on-going. The company would not reveal its own independent design, but is willing to support the project in other ways such as standardisation of the protocol and reviewing the different designs. Another company will likely adapt the PCI Express FMC carrier to

use the PXIe bus and republish this design under the CERN OHL. This new card will be able to profit from all FMC mezzanine cards and the associated firmware and software developments too.

Finally, for the first tender process for CERN of the production and support of 70 PCIe FMC carrier cards, out of the seven companies requested, five did reply. These companies, all having already PCIe products in their catalogue, indicated that they would like to produce extra and sell them as a product of their own, exactly as was intended by the Open Hardware paradigm and licence. Actually any company, even if it did not win the contract, may produce the designs, stimulating a competitive environment. As it is likely that the FMC mezzanine cards will be produced by different companies than those producing the carriers, the Open Hardware concept may promote cooperation between companies.

One of the first designs in the Open Hardware repository is the nanoFIP, an interface chip for the WorldFIP industrial fieldbus. It is likely that this FPGA, that replaces an obsolete commercial device, will be used by a company to renovate a WorldFIP installation inside a train. Also for this company the full availability of the design information is crucial.

FUTURE WORK

As more and more projects are using the OHR, it will be important for engineers to be able to easily find designs for re-use. Currently a simple text based search is possible, but this may not be enough once hundreds of designs are available. The quality of the projects in the OHR will also be important. Already now some projects are very complete and active while other projects have only little information available. Currently this is covered by a status field that shows if a project is in planning state, mature, in alpha, beta or released. This may not be enough.

To allow sharing of design information such as schematics and the PCB layout, it should be possible for everyone to use the same tools that were used to generate this information. We believe that there are currently no free, open tools that are usable enough to make very complex designs and therefore we are looking into possibilities to raise one of the existing free tools to the required level, or to develop another one. Similarly we are helping to add VHDL support to the Icarus Verilog simulation and synthesis tool. Of course these developments will be made with the Open Software paradigm and we hope to attract other interested engineers to help in doing these developments.

CONCLUSIONS

The BE-CO Group at CERN is responsible for electronics that needs to be supported for tens of years. In some cases commercial hardware can be used but has the disadvantage of being black boxes that can only be supported by a single company.

By developing Open Hardware the designs function exactly how we need and in principle anyone can make improvements. Outside specialists may help and the peer review gives the potential for having really good designs. Also one is not tied to a single company for the production and support.

The CERN Open Hardware Licence paved the way for a solid legal ground, while the developed ohwr.org site allows engineers from different sites to easily collaborate on designs and to make the information public.

Having started with designs based on well-established standards such as VME64x, PCIe, FMC and the FPGA-internal Wishbone bus has helped to attract users and to make modules that are easily re-usable.

Finally, it has been shown that small engineering businesses find good opportunities to participate in the design efforts, while companies of various sizes have shown interest in producing and supporting Open Hardware designs in the same way as their own products.

Almost three years of experience show that the OHR environment and the ideas of Open Hardware are stimulating to engineers as it allows the sharing of their knowledge and results in better quality and better documented designs. For companies it gives new opportunities that may need to change their way of operating.

Designed using the Open Hardware concept, the PCIe carrier and 100 MSPS ADC mezzanine are being produced by industry, ready to be installed in CERN's control systems in early 2012. The nanoFIP fieldbus interface chip is also finished and is being designed into control systems. The public nature of this design attracted a European company to re-use it. Other modules, such as the VME64x carrier and 100 kSPS ADC, fine delay and TDC mezzanines are available as working prototypes and will be produced and supported by industry. This base set of modules, together with the supporting IP modules and drivers that have been made will allow rapid development of other modules that will be required by CERN's control systems and those of other installations.

REFERENCES

[1] ANSI/VITA 1.1-1997, VME64x Extensions
[2] PICMG 1.3, System Host Board PCI Express
[3] ANSI/VITA 57.1-2008 (R2010), FPGA Mezzanine Card (FMC) Standard
[4] WISHBONE, Revision B.4 Specification, OpenCores, 2010, http://opencores.org/opencores,wishbone
[5] P.Alvarez et al., FPGA mezzanine cards for CERN's accelerator control system, ICALEPCS 2009
[6] ChiliProject, https://www.chiliproject.org/
[7] Open Hardware Repository, http://ohwr.org/
[8] CERN Open Hardware Licence, CERN, 2011, http://ohwr.org/cernohl
[9] http://freedomdefined.org/OSHW