FPGA-BASED HARDWARE INSTRUMENTATION DEVELOPMENT ON MAST*

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Abstract

On MAST (the Mega Amp Spherical Tokamak) at Culham Centre for Fusion Energy some key control systems and diagnostics are being developed and upgraded with FPGA hardware: real-time data acquisition, vertical stabilisation, resonance mode driving, laser triggering, fast timer prototype, neutral beam monitoring and the bolometer upgrade. FPGAs provide many benefits including low latency and real-time digital signal processing. We accomplish lower costs by using industry standards such as the FMC (FPGA Mezzanine Card) Vita 57 standard [1] and by using COTS (Commercial Off The Shelf) components. Abstracting of the design and by using a flexible FPGA architecture gives resistance to obsolescence of modules and the ability to upgrade easily to add functionality by changing individual modules (connected by standard interfaces), avoiding the need to change the whole system.

FPGA DEVELOPMENT ON MAST

FPGAs are becoming more widely used in fusion research. In conjunction with appropriate hardware (DACs, ADCs, communication interfaces, etc) they offer a large number of capabilities including timing synchronisation, triggering, analogue/digital processing, I/O control, real-time feedback, embedded processors and more. As such this paper discusses this technology presented as a "standard architecture" where some systems (Resonance Mode Driving and Detection, Vertical Stabilisation, Real-Time Fast Acquisition, Fast Timer Prototype, NBI) use this architecture.

STANDARD ARCHITECTURE

MAST like other experimental facilities is a place where researchers are continually interested in investigating newly discovered phenomena. In order for researchers to be effective in this aim, it is necessary to have flexible hardware which allows researchers to adapt the system to the needs of their experiments. In many cases purchasing "turn-key" solutions to a cutting edge research experiment is either not possible or very expensive. We accomplish lower cost and flexibility instead by using a standard architecture that has the aim of being cost effective, flexible and reliable. By using open standards (Gigabit ethernet, FMC, SPI/IIC, AXI, ST Optical Fiber) it makes it easier to use different components of a system (such an FMC ADC board) in a variety of systems. This makes it easier to develop new systems, maintain and upgrade existing systems.

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RESONANCE MODE DRIVING AND DETECTION

Toroidal Alfvén Eigenmodes (TAE) are global plasma modes at frequencies of 80 to 120 kHz. These eigenmodes can be considered analogous to orbit beam eigenmodes in synchrotrons and accelerators [2]. In MAST these modes can be driven by Neutral Beam Injection (NBI) or a time varying magnetic field generated by external coils.

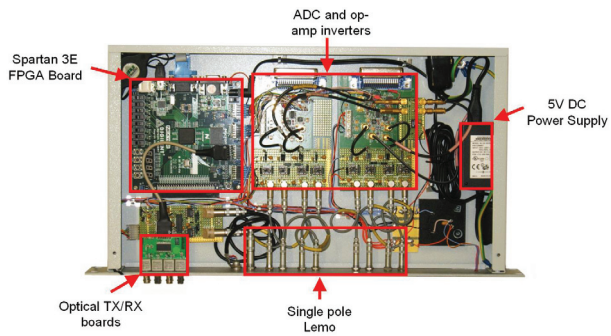

Figure 1: A resonance mode driving and detection system. Toroidal Alfvén Eigenmodes appear at ~80-120 kHz. An FPGA used system is used to create a time varying edge magnetic field perturbation by driving ~10 A sine wave in coils around the edge of the plasma.

The FPGA system (see Figure 1) is designed to drive these external coils. The FPGA creates an analogue sine wave via 16-bit DACs which are swept in frequency from 80 to 120 kHz. The sine wave is modified to have a fast zero crossing which reduces the reflected amplifier power. A ~10 A current is driven in the TAE coils using a matched resonant circuit. Parameters are loaded onto the FPGA using a serial UART connection which is connected to a rack-mounted serial over ethernet device. The benefit of UART is that it provides a low level communication (with a cost of only two wires) which can be used to debug the device. A future upgrade will likely switch this to gigabit ethernet. Additionally a 1 MHz 12-bit ADC can be used to digitise an arbitrary input signal for closed-loop real-time feedback, such as for tracking the resonant TAE frequency in real-time.

LASER TRIGGERING

A laser triggering system developed on MAST [3] is used to trigger 8 Nd:Yag Lasers 1.6 J 33 Hz (peak power 10 MW). The system incorporates a Spartan 3E FPGA with UART communication, fast rise-time triggers, and optical amplitude digitisation. This system is currently being enhanced for physics experiments in closed loop triggering applications to study plasma disruptions and instabilities.

VERTICAL STABILISATION

The Vertical Stabilisation system controls the vertical plasma position by adjusting the voltage in the P6 coils (see Figure 2).

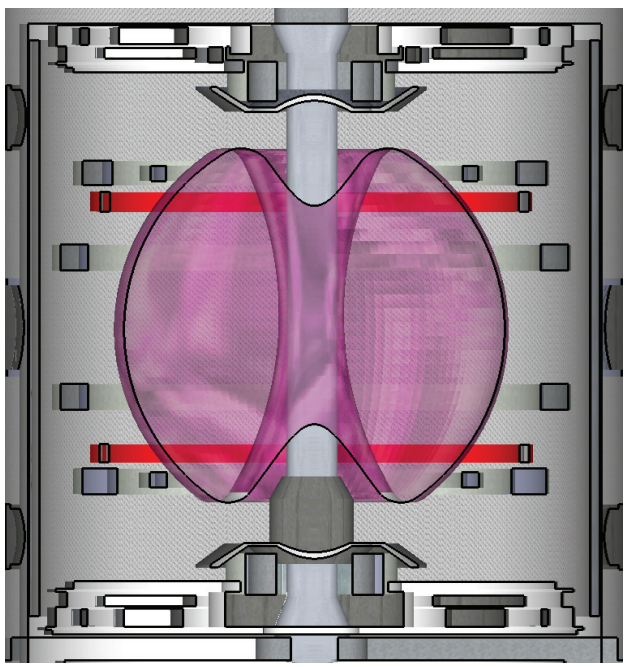

Figure 2: A cutaway view of the MAST vessel. The P6 magnetic coils which control the vertical position of the plasma are highlighted red. The coils are wired anti-parallel and driven by the vertical control system.

Currently an analogue vertical position control system is used to minimise the loop delay. However, there is little headroom between the optimal loop gains and those at which fast plasma events, such as 'Edge Localised Modes', will cause the amplifiers to trip. It is hoped that the use of an FPGA system (see Figure 3) will retain the benefit of low delay while allowing use of dynamic gain control and optimal filtering to make best use of the available dynamic range in the closed loop system.

The system comprises of: SP601 Spartan 6 FPGA, FMC12PEXP LPC Digital I/O, ADS1672 24-bit 625 ksps, remote management board, custom fibre optic boards for trigger/clocking, ATX power supply, 16-bit DAC for waveform generation.

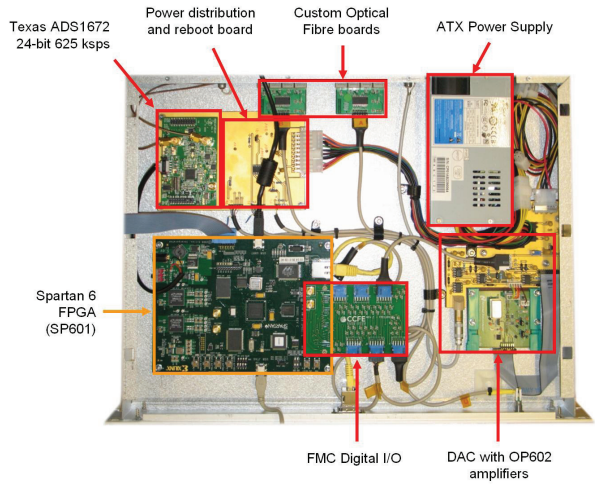

Figure 3: The new digital vertical stabilisation system contains a SP601 Spartan 6 FPGA. Gain coefficients and vertical position waveform are loadable over the Gigabit ethernet.

FAST REAL-TIME DATA ACQUISITION

The Microwave Imaging Diagnostic on MAST requires a fast real-time data acquisition system. Using the AXI bus it is possible to achieve a high continual streaming rate of 8 GB/s. This speed is based on 16 channels acquiring at 14-bits at 250 Msps: $16 * 2\,\text{Bytes} * 0.25\,\text{Gsps} = 8\,\text{GB/s}$. The system has been proved to be capable of achieving acquisition speed of >10 GB/s. This is compared to the theoretical rate of 12.8 GB/s for two DDR3 RAM chips 64-bits wide driven at 400 MHz DDR.

The hardware consists of 2xML605 FPGA Virtex6 boards, with on board 2 GB DDR3 RAM (4 GB Total), 2xFMC108 4DSP 14-bit 250 Msps ADC, FMC12PEXP LPC Digitial I/O, Gigabit Ethernet, Compact Flash, ATX Power Supply and Optical Reboot Board. The SSMC connectors on the FMC108 boards are internally wired to SMA front panel connectors. This is due to the fragility of SSMC (rated only for ~10 on/off connections) compared to the ~500 for SMA.

FAST TIMER PROTOTYPE

On experimental physics devices it is necessary to distribute a common clock to synchronise all instruments. A fast timer prototype (see Figure 4) has been developed to allow synchronisation using a distributed 10 MHz clock and generation of variable delay/length triggers. The system is a 1U system with ATX power supply, remote management board, LPC FMC12PEXP digital I/O, optical clock and trigger boards. The system uses an SP601 Spartan 6 board with Gigabit ethernet for communications. The generated pulse has a 37 ns precision with ~4 ns jitter. On board parallel (BPI) flash to store the firmware to makes this system fully standalone (the network is not needed for booting).

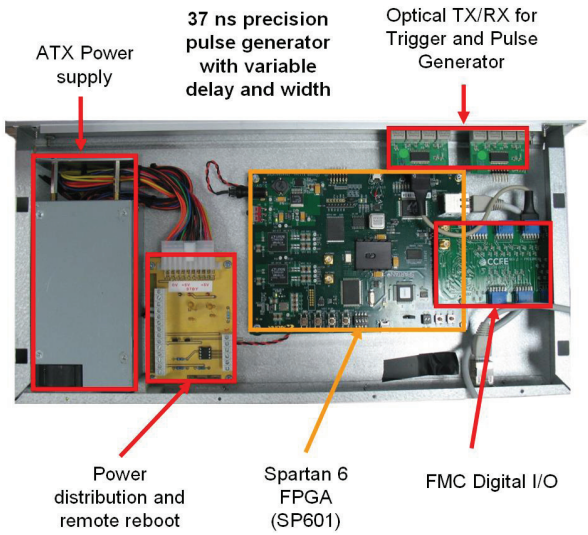

Figure 4: The Fast Timer Prototype. A simple system that contains many aspects of the FPGA standard architecture showing the ease with which new diagnostics and control systems can be developed. It is a completely remote managed system that communicates over ModBus.

NBI FPGA DIAGNOSTIC

The Neutral Beam Injection (NBI) system on MAST injects over 3.2 MW of power into the tokamak. As part of the running operations there are occasionally arcing currents. Currently these are monitored at 20 kHz sampling rates but since arcs can happen over smaller timescales than 50µs. This new system (see Figure 5) will include: 4 Channel 1 Msps 12-bit ADC, ATLYS Spartan 6 FPGA, ATX power supply, remote reboot board.

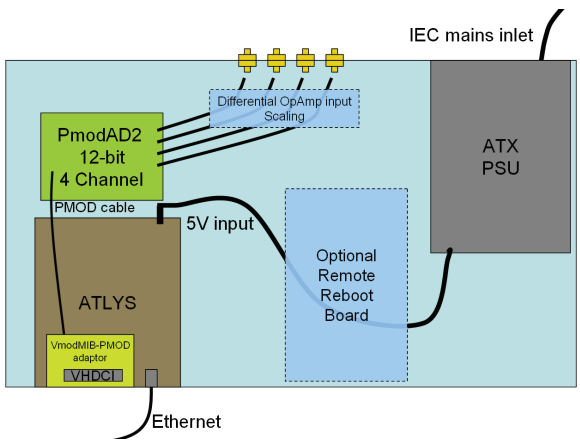

Figure 5: The NBI arc detection acquisition system. This system increases the sampling rate from 20 kHz to 1 MHz in order to better resolve the voltage waveform during an NBI arc event. This system utilises an ATLYS Spartan 6 board and follows the FPGA standard architecture.

BOLOMETER UPGRADE

The bolometer array is a 32 channel system on MAST which measures plasma irradiation from visible to soft X-ray. The detection system is based on gold foil configured as a wheatstone bridge whereby incident radiation causes a voltage difference across the bridge.

The challenge with this system is that in any given time interval a very small amount of power falls onto the gold foil thus making the diagnostic sensitive to noise. An additional requirement is low temperature drift. In order to increase the sensitivity of the system and help prevent problems with low DC offsets and 1/f noise a chopping sine wave at 20 kHz is used. The hardware will be FPGA based to control the calibration of the wheatstone bridge, digital filtering, control waveform and other control operations.

CONCLUSIONS

Significant FPGA development is occurring on MAST in key control systems using a standard FPGA architecture. The adoption of a standard architecture has enabled the development of a number of different diagnostics performing a variety of different functions.

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