STATUS OF THE CONTROL SYSTEM FOR THE EUROPEAN XFEL

K. Rehlich, DESY , Hamburg, Germany

Abstract

DESY is currently building a new 3.4 km-long X-ray free electron laser facility. Commissioning is planned for 2014. The facility will deliver ultra short light pulses with a peak power up to 100 GW and a wavelength down to 0.1 nm. About 200 distributed electronic crates will be used to control the facility. A major fraction of the controls will be installed inside the accelerator tunnel. MicroTCA was chosen as an adequate standard with state-of-the-art connectivity and performance including remote management. The XFEL [1] will produce up to 27000 bunches per second. Data acquisition and controls have to provide bunch-synchronous operation within the whole distributed system. Feedbacks implemented in FPGAs and as service tier processes will provide the required stability and automation of the FEL. This paper describes the progress in the development of the new hardware as well as the software architecture. Parts of the control system are currently implemented in the much smaller FLASH FEL facility.

INTRODUCTION

The front-end electronics will be distributed along the 3 km long machine. Since a major part of the XFEL is running below populated public areas, the electronics has to be placed inside the tunnel close to the accelerator components. This requires appropriate shielding against radiation and remote management capability of the hardware. Furthermore, shots will have repetition rate of 10 Hz and a length of a ms. The bunches are spaced with 1/4.5 MHz and 27000 bunches per second have to be recorded and processed. A timing system is planned to synchronize all front-end systems. Data of all subsystems will be transmitted to central services and have to be sorted to sync all bunches. A fast DAQ system, designed and operated for FLASH [2], will provide a common solution for multiple services. As common hardware platform MicroTCA has been defined as the standard for XFEL fast controls.

MICROTCA STANDARD

Hundreds of megabytes per second have to be transferred within a crate and to the central services. MicroTCA provides these fast transfer rates and offers GigaLinks as point-to-point connections between modules for e.g. fast feedbacks. And MicroTCA has a very well defined interface to manage crates and individual modules. This is described in the next chapter.

But, the original specification was driven by telco applications. Analog IO and the distribution of timing information were not foreseen. Therefore a group of laboratories together with industrial partners initiated a working group within the PICMG ® [3] to specify rear

transition modules, clock and trigger distribution. One result of this committee is the MTCA.4 specification, which is available since October 2011. It is fully compatible to the older MicroTCA specification. All existing modules can run in this new extended standard. During the specification period institutes and industry have designed first prototypes.

The driving idea of this MTCA.4 standard is to build only a few complex front modules as AMCs (Advanced Mezzanine Cards) and many simple RTMs (Rear Transition Modules) to adapt the AMCs to different applications. AMC and RTM are connected by two shielded 30 pair ADF connectors. They support fast GigaLinks as well as sensitive analog signal transmission. Six pairs of one plug are defined as management and power interface of the rear module. RTMs are fully integrated in the crate management. Hot-swap as well as a protection against wrong inserted modules are defined.

In September 2011 DESY has successfully demonstrated a MicroTCA system controlling one super-conducting RF module, with 8 cavities, driven by one 5 MW klystron. The Low Level RF system (LLRF) was completely installed in a MicroTCA crate according to the MTCA.4 standard.

The setup was (Figure 2):

- Three 125 MSPS, 16 bit ADCs with 1.3 GHz down-converters as RTMs.
- One controller with a vector modulator to drive the klystron.
- One timing module to synchronize the LLRF with the linac.
- A CPU and disk.
- An MCH as a switch for Ethernet and PCIe and to manage the crate.

It was shown that MTCA.4 can operate sensitive analog
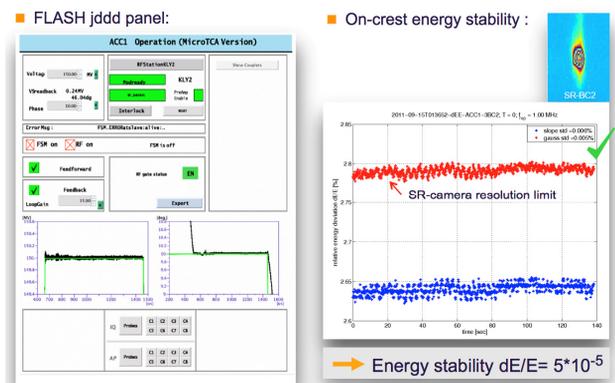
Figure 1: 800µs flat-top operation of FLASH with the new µTCA system.

electronics together with high frequency switched digital CPUs and FPGAs without degradation of signals quality.

The measured energy stability of the FLASH electron beam during 800 µs was better than $5*10^{-5}$ (Figure 1). This fulfills the XFEL requirements.

This demonstration included the full chain of new developed firmware, Linux drivers, DOOCS device servers and hardware management. In other words, the MicroTCA crate was completely integrated into the control system of FLASH. The device servers were written in a way that existing client programs find many names of the old VME system and required only minor modification to address new features.
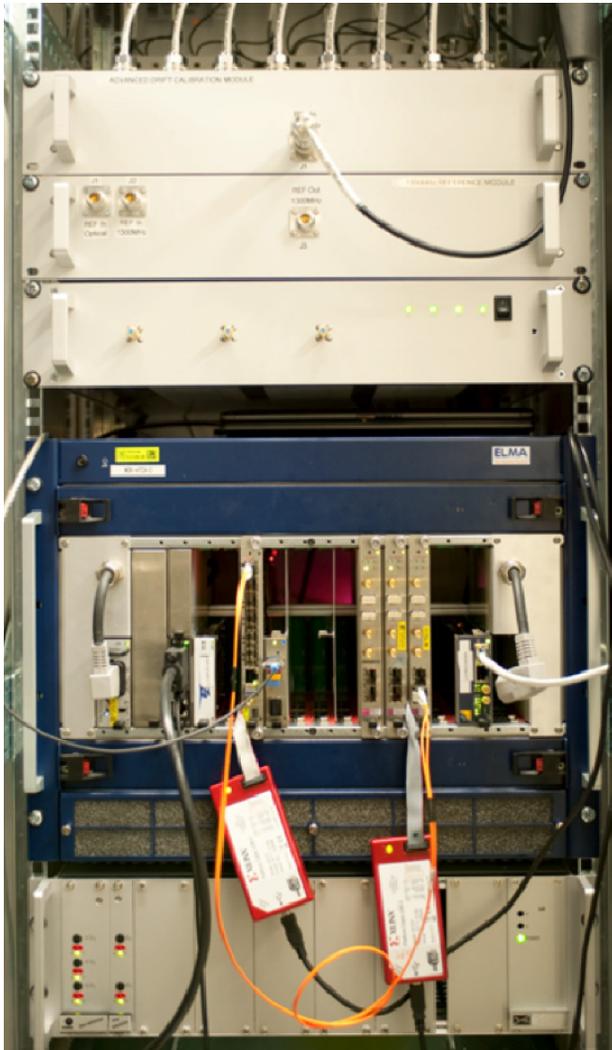
Figure 2: The rack with the blue MicroTCA crate controls 8 superconducting cavities of one cryo module in FLASH.

HARDWARE MANAGEMENT

The hardware management operates on two levels. IPMI commands are available on the MCH Ethernet port for remote access. And within a crate PCIe is used to handle hardware events.

MicroTCA specifies IMPI functions for all hardware modules in a crate. It includes all AMC modules, fans, and power supplies. A DOOCS server, as a middle layer service, talks to all crates and dynamically detects inserted modules and monitors them. If a user inserts an AMC module the server creates a device instance for the module. It allocates data archives for the voltage and temperature readings and creates the corresponding addresses to be accessible for clients (Figure 4). During configuration of the server it is just required to specify the crate IP address, the other information is read from the hardware via well-defined IPMI commands. Furthermore, rebooting of a CPU with a frozen operating system can be initiated by power cycling an AMC via the IPMI DOOCS server.

Within a crate the PCIe signaling allows to handle removal and insertion of modules. In a running system one can remove e.g. one ADC board. The DOOCS server continues with the other ADCs and marks the removed one as faulty. After reinsertion of the ADC the server restores the registers and continues readout. This hot-swap does not require any operator actions. Linux drivers and DOOCS server processes automatically handle it.

MIDDLE LAYER SERVICES

As mentioned, XFEL will produce up to 27000 bunches per second. A data acquisition system (DAQ) has been implemented at FLASH to cope with the high data rates and to synchronize the data from a distributed system in one or more middle layer servers. The system is used for online processing of bunch related data, to archive all bunches of all monitors, and to store data of user experiments of the photon beam lines.
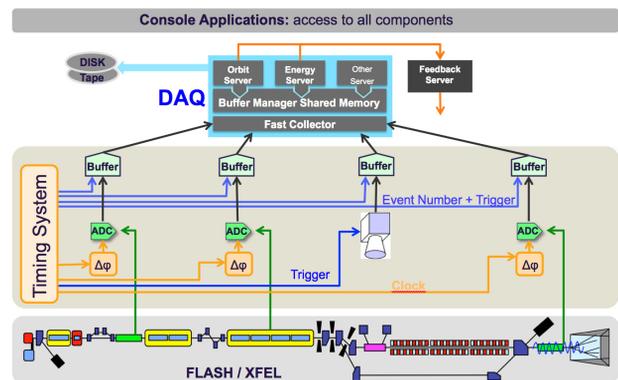
Figure 3: The timing system synchronizes the distributed controls. Data is collected in the central DAQ system.

The DAQ provides data of all BPMs for instance to calculate an orbit. This service was recently used to attach a slow orbit feedback to stabilize the beam in all sections of the accelerator (Figure 3). As a display and configuration tool jddd was used.

These three software packages, the DAQ, the feedback process and the jddd panel editor [4] are components to be used for XFEL commissioning. FLASH is used to test

the new hardware and software. Both, FLASH and XFEL will profit from this parallel development.

CONSOLE APPLICATIONS

The graphical operator panel design tool jddd is a further development for both machines. The goal of the design is to create a tool that is simple and can be used without knowledge of programming languages. Operators and subsystem experts are able to create themselves panels and can run them on multiple platforms. Jddd is Java based and the panels are stored in a Subversion repository. The panel can run on Mac OS, Windows and Linux operating systems.

Although jddd is usable without writing code, it has many complex widgets to construct highly dynamic panels. For example displays showing all running processes of the control system were created. During run-time these panels are dynamically updated by reading from a name server and device servers. See [4] for more information.

CONCLUSIONS

MicroTCA has been chosen as the standard platform for the XFEL. A first implementation of the LLRF controls based on this new standard has demonstrated that the most complex subsystem could be realized with excellent performance. This is a proof of principle for the new MTCA.4 standard. All required hardware and software components could be implemented and successfully tested. It includes hardware design, firmware, module management, Linux drivers, control system device servers and high level management server and display.

ACKNOWLEDGEMENTS

This work was only possible with the excellent contributions of many members of collaboration partners from Poland and Sweden, industrial partners, and the DESY groups MSK and MCS4 – many thanks to all of them.

REFERENCES

[1] http://xfel.desy.de

[2] http://flash.desy.de

[3] PICMG, http://www.picmg.org

[4] http://jddd.desy.de
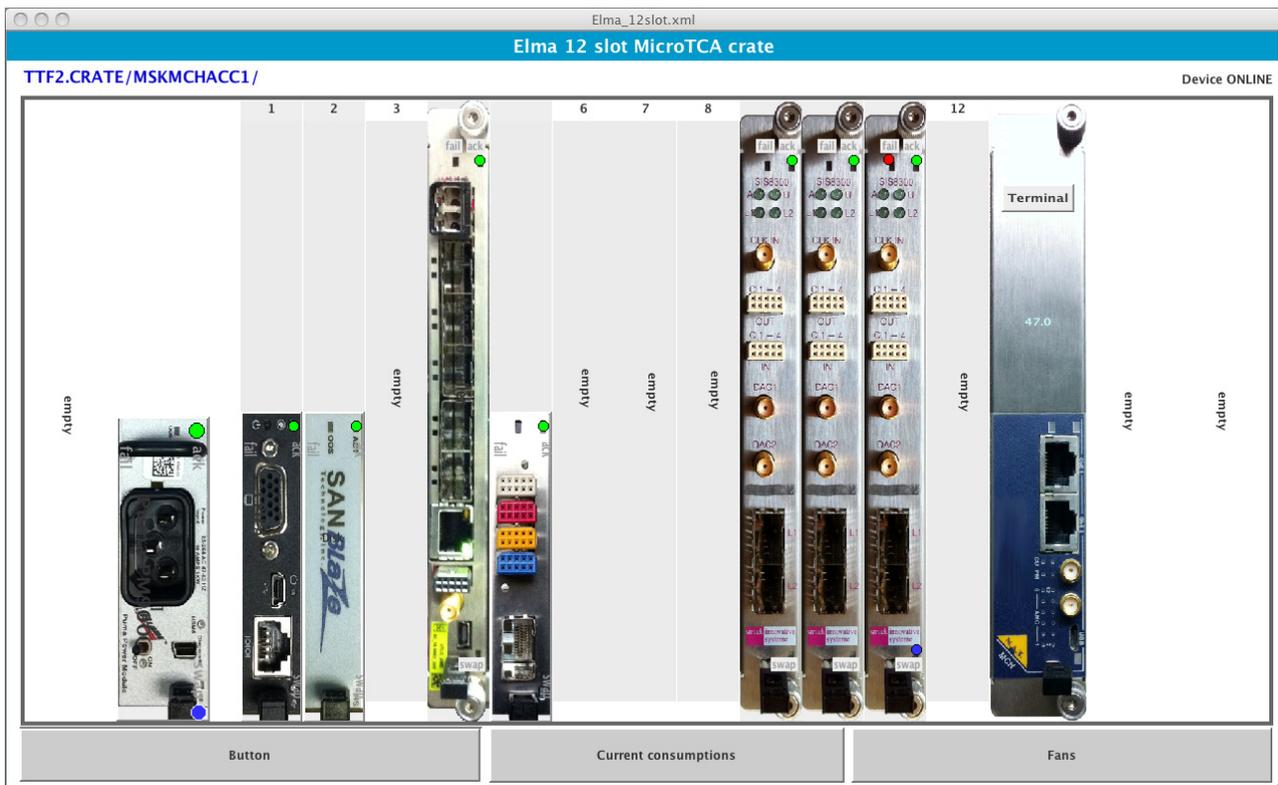
Figure 4: The MicroTCA crate displayed by jddd. A click on a module starts a panel with further details.