THE MICROTCA ACQUISITION AND PROCESSING BACK-END FOR FERMI@ELETTRA DIAGNOSTICS*

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Abstract

During the construction and commissioning of the FERMI@Elettra Free Electron Laser (FEL) facility, tight requirements for diagnostics readout, processing, and control electronics had been specified; together with a complete integration in the main machine control system. Among the diagnostics devices to be controlled, the Bunch Arrival Monitors (BAM) [1] and the Cavity Beam Position Monitors (C-BPM) [2]. The back-end platform, based on the MicroTCA (or uTCA) standard [3], provides a robust environment for accommodating such electronics, including reliable infrastructure features for slow control and monitoring of the electronics inside the crates. Two types of Advanced Mezzanine Cards (AMC) had been conceived, developed and manufactured in order to meet the demanding requisites. The first is a fast (160 MSps) and high-resolution (16 bits) Analog to Digital and Digital to Analog (A|D|A) Convert Board, hosting two A-D and two D-A converters controlled by an FPGA. The onboard logic is also responsible for service and host interface handling. The latter board is an Analog to Digital Only (A|D|O) Converter, derived from the A|D|A, with an analog front side stage made of four A-D converters. Timing synthesis and distribution from a MicroTCA Central Hub (MCH) slot can be provided by means of a custom MicroTCA Timing Central Hub (MiTiCH), specifically designed for accurate (sub ps range) timing distribution over uTCA backplanes. The overall systems' architectures, together with the AMCs and MCH concept and functionalities, are described hereafter. A summary of the achievements, for each specific use case, together with our experience in the field with the new architecture, are then summarized.

SYSTEMS GENERAL REQUIREMENTS

In spring 2009 a team specialized in digital electronics had been put together by the area leader of the FERMI timing and diagnostics, to develop a common acquisition and processing platform to be interfaced to the machine control system. The goal of the diagnostics uTCA crates, named back-end systems, was to cover the control of 25-30 stations spread along the machine in both the linac and the undulator areas. The ADC count summed up to about 100 inputs, while the DAC output had been estimated to 40 in groups of two fast and two slow converters. Extra general purpose IO capabilities for control and monitor had also been requested.

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The need for a modular system was therefore obvious. The main facility objective was to lase 19 months later; consequently the development was to be kept realistic, yet innovative because of its tight constraints. After a survey of suitable system architectures, the choice for uTCA was made. Even if very attractive, xTCA for physics was at the time still in its embryonic stage. Designer decided to avoid commercial solutions for two reasons: (i) none of the offers were fulfilling all systems' criteria and the numbers in play wouldn't attract vendors to customize their products; (ii) none had the desired degree of openness required to truly operate, maintain and upgrade such devices. A custom or open design is intrinsically, from hardware to software, under complete control of developers. Costs and manpower were properly scaled to cover the effort required to start with uTCA. The standard had been chosen for its modularity and size, its backplane bandwidth capabilities, and the robustness of modules' supervision. Of fundamental relevance also the fact that MicroTCA had the scalability and the potential for future expansion, characteristics desired by the designers during the conception stage.

BACK-END OVERVIEW

The uTCA back-end system (Figure 1) is a hardware layer interface between the tunnel frontend devices, specific for each diagnostics monitor, and the machine control system. The communication to/from frontends is application dependant; while the data transfer to the control network devices is Ethernet UDP/IP based. Users in the control room can monitor and control devices through Linux real time and Tango servers and panels. Inside the uTCA the clock can be distributed via the backplane, while all other signals are connected via front panel connectors.

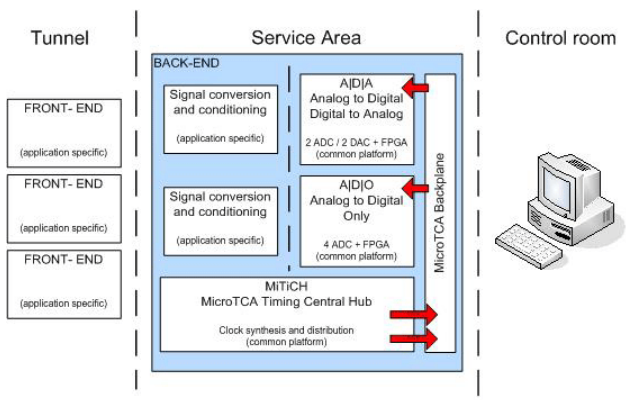

Figure 1: Block diagram of a diagnostic back- end system.

Besides Commercial Off-The-Shelf (COTS) devices like Shelf Managers, CPUs and hard drives; the uTCA back-end crate is conceived to host three types of modules: (i) **A|D|A and A|D|O AMCs**, custom modules described later in this article; (ii) **Side Transition Modules (STM),** interface transition cards (in AMC format) that adapt front-end signals to the inputs and outputs of A|D|A and A|D|O, and communicate with them through fine pitched flat cables; (iii) **Clocking and shelf management MCH**, MiTiCH like modules for card monitor and/or clock distribution.

A|D|A MODULE ARCHITECTURE

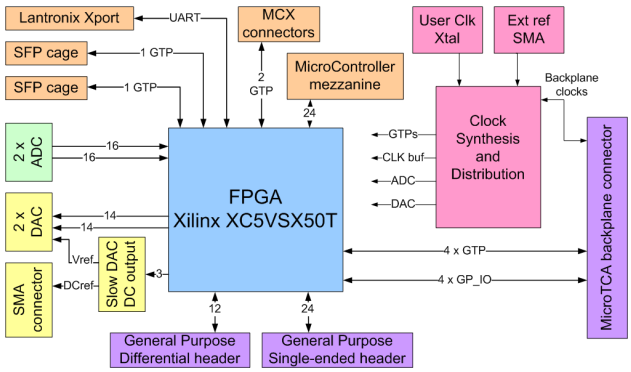

Figure 2: A|D|A AMC module block diagram.

The main purpose of the Analog to Digital and Digital to Analog (A|D|A, Figure 2) converter AMC [5] is acquisition, processing, and generation of fast analog signals. The architecture is based on a Xilinx Virtex-5 FPGA responsible for the data handling of all the external inputs and outputs, the data processing, and the interface to the control system. Extensive board documentation can be found in [6].

A|D|O MODULE ARCHITECTURE

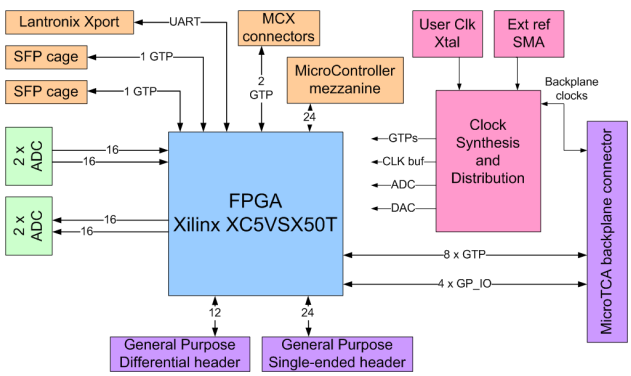

Figure 3: A|D|O AMC module block diagram.

The Analog to Digital Only (A|D|O, Figure 3) converter AMC [7] is derived directly from A|D|A. It is based on the same FPGA responsible for the same generic tasks. The main difference between the two cards is the front-end that in the A|D|O case in made of 4 A-D converters. The backplane connectivity and the clocking schema has both been enhanced and improved.

MITICH MODULE ARCHITECTURE

MCH Carrier Board

The uTCA standard specifies [3] the delivery of power on a backplane connector (tongue 1) physically separated from the one devoted to clock distribution (tongue 2). The development of a base board to provide power to the clock card was therefore necessary (Figure 4). The availability of space on the base board allowed the implementation of additional test features, extender like, for backplane high-speed connectivity characterization. Evaluation of the I^2C control bus for Intelligent Platform Management Interface (IPMI) [4] used for shelf management in uTCA systems had been also predisposed.

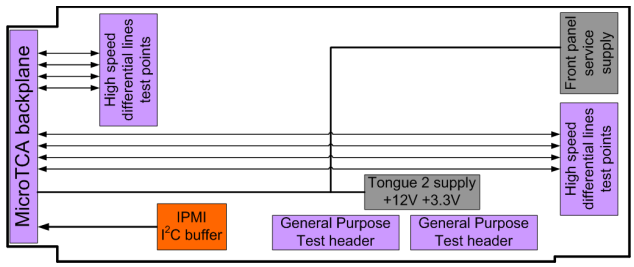

Figure 4: MiTiCH MCH tongue 1 block diagram.

MiTiCH Block Diagram

MiTiCH is a MicroTCA Timing Central Hub (Figure 5) [8] compliant to the uTCA mechanical specifications for MCH tongue 2. Its purpose is the synthesis and distribution of clock signals. To enhance its flexibility, a future revision of the card will host a vector modulator for RF phase control up to S-Band. The key component is an AD9516-4 frequency synthesizer, controlled by a microcontroller, interfaced to the network via a Lantronix. Two stages of fanout buffers distribute two frequencies to up 12 AMC modules on the backplane.

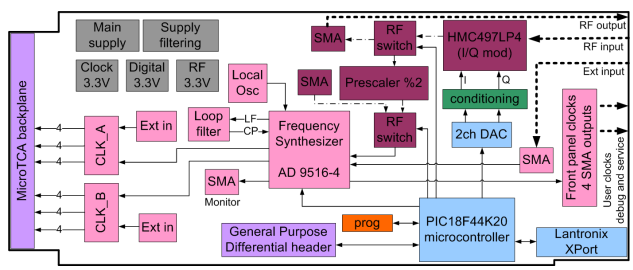

Figure 5: MiTiCH MCH tongue 2 block diagram.

The Charge Pump feedback filter circuit of the PLL can be tuned onboard changing its passive elements; alternatively the internal VCO can be controlled with an external voltage. Characteristics of the circuit can by comfortably studied with the Analog Devices ADIsim-CLK™ tool. Frequencies can be derived either from internal oscillators or external references.

FIRMWARE AND CONTROL SOFTWARE

The idea behind the **firmware** architecture (Figure 6) for both the A|D|A and the A|D|O cards is to provide black box core logic to support a user space containing application specific functions. Three blocks had be identified and developed separately. (i) The control and monitoring block interfaces the card to the controls network. Data flows through an internal memory mapped RAM based space, providing an independent and well defined separation between the different blocks. (ii) The interface layer consists of a series of buffers controlled by state machines collecting and storing data to and from the digitizers. (iii) The clock and timing section exploits digital clock management.

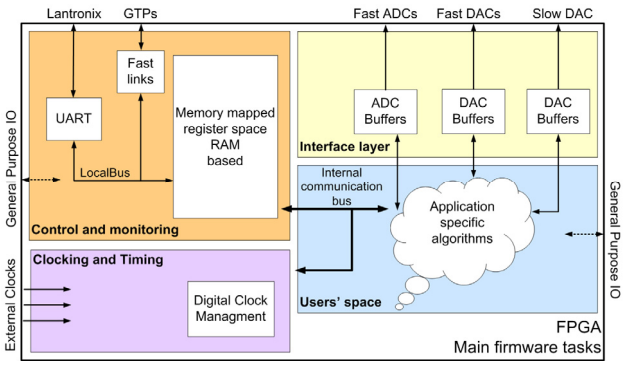

Figure 6: block diagram of the firmware sub-modules.

The **control network** bunch-by-bunch acquisition system for both monitors is based on VME PowerPC field stations. Each crate hosts a MVME7100 board running Linux with the Xenomai realtime extension and Tango control system software. One of the four Gbit Ethernet ports onboard is reserved for A|D|O and A|D|A communication. Upstream, at each machine shot, the AMCs acquire information from the field and transmit it to the control system via UDP/IP. A Xenomai real-time task running at the kernel level extracts from a dedicated Ethernet port, directly from the interrupt handler, the UDP data payload and performs further computation. A Tango server exports to the control system level the information collected by the real-time task. Downstream, a Tango server can interact with hardware; e.g. in the C-BPM case two slow loops regulate the amplitude of calibration signals and the gain level of analog front-ends.

BACK-END SYSTEMS COMMISSIONING

During the commissioning of the FEL, the diagnostics monitors based on the uTCA back-end were installed and put into operation. The following paragraphs will describe each specific application goal and achievements.

The BAM Case

Figure 7 shows a block diagram of a complete BAM station. In this setup, the back-end enclosed in a 1U uTCA crate consists of: one A|D|A, 1 Signal Conditioning Board (SCB) STM [1], and two 12 GHz photo-diodes.

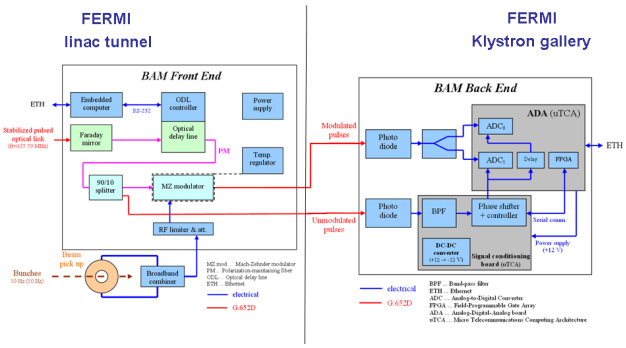

Figure 7: BAM system architecture.

The goal was to deliver three stations to characterize the FEL measuring its beam arrival time in strategic locations, with an accuracy of less than 20 fs. Major problems due to EMI interference inside the uTCA crate, forced designers to split the functionalities in separate crates. A custom chassis hosting the SCB and the Photodiodes had been therefore built. Installing two stations the goal of demonstrating the system principle was accomplished successfully, and an average system resolution of 7.66 fs was confirmed. Using BAM stations, measurements of the machine bunch compressor and some studies on the linac stability performance are now routine tasks of operators.

The C-BPM Case

In order to operate a C-BPM station the following modules are required: one A|D|A, one A|D|O, one MiTiCH, one OptioIO STM [2]. In this configuration, the back-end system enclosed in a 9U uTCA crate can host up to 3 C-BPM stations (Figure 8). The MiTiCH and one of the two A|D|A are shared between two monitors. The goal set was the delivery of 10 stations to operate the FEL with a beam position measurement of 1 um or better.

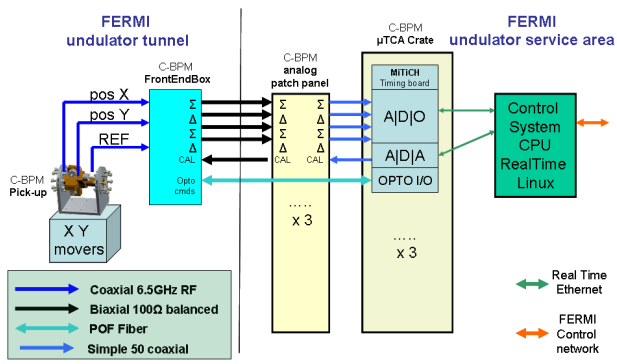

Figure 8: C-BPM system architecture.

EMI problems caused by the uTCA original 220 VAC PSU forced its replacement; no other issues were experienced in this case. All planned systems were installed and successfully commissioned delivering monitors with an average resolution of 1.7 um. Exhaustive documentation on system calibration and position calculation can be found in [9] and [10].

To meet the final resolution specification, further fine tuning of the frontend electronics is planned. The instruments had been of fundamental importance to transport the beam along the undulator chain to achieve FEL light in December 2010. Beam transport and fast trajectory feedback [11] are now control room routine operations based on these devices.

OTHER UTCA DEVELOPMENTS

For future system enhancement and to fulfil complete standard compliancy, other system features were tested. Figures 9-10 show a schematic view of two uTCA advanced functionalities:

1. Intelligent Platform Management Interface (IPMI)
2. Fast backplane connectivity to a CPU via PCI Express

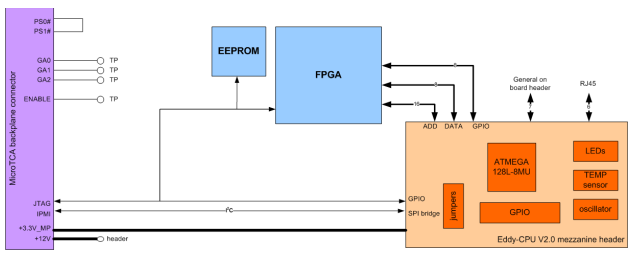

Figure 9: IPMI AMC controller .

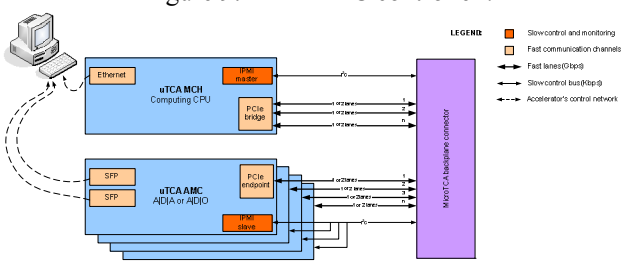

Figure 10: Fast AMC connectivity.

In collaboration with DESY in the framework of the IR-UV-X EuroFEL-PP, the above tasks were successfully carried out on an intensive measurement session at Elettra. (i) An Atmega 128L-8MU evaluation kit, wired to and A|D|O, proved the capability of the board to communicate to a commercial N.A.T. MCH for shelf management: hot swap and basic current and temperature readout and monitor were performed. (ii) A|D|O was successfully capable of transferring and receiving data via PCI Express to an ADLink CPU AMC1000 (Intel x86 64bit) and Sanblade SATA HDU, at a rate of 4 lanes at 2.5 Gbps (10 Gbps). The operating system and drivers used for the test were Linux based.

FIELD EXPERIENCE WITH UTCA

In general, the choice for uTCA as system architecture had been proved to be correct. It is a robust and reliable platform (5 machine runs without faults) handy to service and maintain. Especially working in the laboratory with its advanced functionalities, we had the chance to thoroughly explore the technology's potentials. EMI weakness in the crates evaluated were unexpected. Never the less the problems have been tackled and solved. We hope, especially in view of the physics extension (xTCA), that extra care on those issues will be taken by crate manufactures. We firmly believe that uTCA as is, will remain a valuable alternative for small scaled systems or modular systems were integration on AdvacedTCA (ATCA) blades is possible.

CONCLUSIONS AND OUTLOOK

Presently all systems required to operate the first FEL line (FEL1) of FERMI had been successfully installed and almost all commissioned. The total number of cards produced and tested sums up to 24 A|D|A, 18 A|D|O, and 4 MiTiCH. The number of uTCA crates on the field is 6. Those numbers will soon grow as the second FEL line will be commissioned. The platform and its modules are solid foundations for R&D in the digital electronics domain that we wish will continue also in the future.

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