DEVELOPMENT OF IMAGE DATA ACQUISITION SYSTEM FOR 2D DETECTOR AT SACLA

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Abstract

We have developed a data acquisition system for X-ray and optical imaging devices at SACLA (SPring-8 Angstrom Compact free electron LAser). The frontends with the Camera Link interface transfer the data to data-handling servers, which buffer and distribute the data to on-line monitors and a high-speed storage. The system is partly operational for SACLA beam commissioning since March 2011. The full system for X-ray 2D detector experiments will be released in November 2011.

INTRODUCTION

The X-ray free electron laser (XFEL) facility, SACLA, has been constructed at the SPring-8 site. The XFEL has unprecedented characteristics such as high peak brightness, ultra-short pulses, and full spatial coherence. These features are believed to open new opportunities in a variety of scientific fields. The facility has started to accelerate electron beams up to 8 GeV in February 2011, and the first X-ray laser was observed in June 2011.

In order to meet the requirements of proposed experiments to be performed at SACLA, Multi-Port Charge-Coupled Device (MPCCD) detector has been developed. The MPCCD sensor has 0.5 M pixels with 50 um square pixels. It is packaged in a 4-side buttable arrangement in order to enable large area detector by forming tiled array [1]. In the first experimental runs starting from March 2012, two arrayed detectors with 8 and 4 sensors in tandem will be the operation with maximum data rate reaching 5.8 Gbps. Each sensor is driven by a readout board, which transmits the digitized data through a Camera Link base configuration interface. The resulting data is processed on the VME Camera Link board, and transferred to a data-handling server via TCP/IP socket communication on 1 Gbps Ethernet. The data are pipeline buffered on the server, and sent to the on-line data visualization terminals, and a data file server connected to the high-speed data storage. The data acquisition is carried out completely in parallel so to ensure the scalability for detectors with arrayed sensors.

FRONTEND

We have developed the image data-handling scheme using the event-synchronized data-acquisition system [2]. We selected the Camera Link standard to achieve real-time triggering and high-speed data transfer. We have made available a VME Camera Link board for base configuration cameras in addition to the off-the-shelf PCI-express Camera Link board (AVALDATA APX-3318) for medium and full configuration devices. The former board has been developed in order to achieve on-the-fly lossless compression.

VME Camera Link Board

The VME Camera Link board is composed of a Camera Link base configuration interface and a processor PMC (PrPMC) mezzanine cards onto a carrier VME board with a FPGA [3]. Figure 1 shows VME Camera Link board. The data is first acquired via the Camera Link interface card and sent to the FPGA, Virtex-5 FXT (XC5VFX70T), and buffered to a DDR2 memory. Buffered data are compressed by a lossless range-coder algorithm within the FPGA, and transmitted to the buffer in the SDRAM on the PrPMC card. On the PrPMC card, TCP/IP socket server process is running on Freescale Semiconductor embedded Linux. A client process on the data-handling server receives the data through a Gigabit Ethernet interface. The achieved overall data rate in this scheme was 760 Mbps, which outperforms the required bandwidth of 480 Mbps. The carrier board has another Gigabit Ethernet interface. The Linux hard core on the FPGA has another TCP/IP socket server process on the TimeSys Linux, which can deliver the uncompressed data at the reduced frame rate for on-line monitoring. The measured data rate was 200-300 Mbps. Currently we have implemented MPCCD detector and a VGA camera for the screen monitors of the beamline.

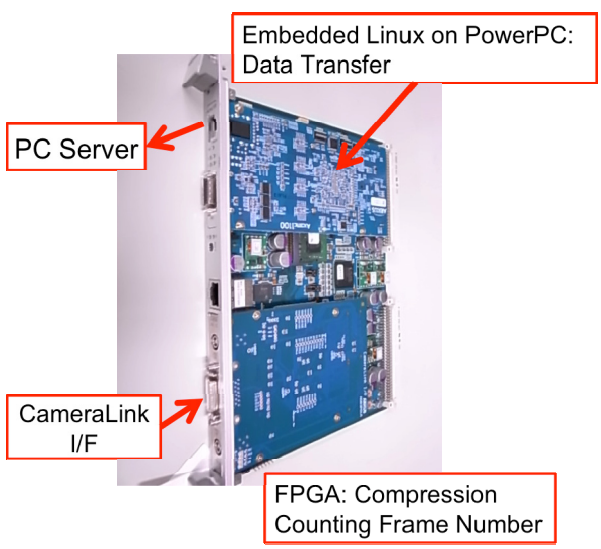

Figure 1: VME Camera Link board.

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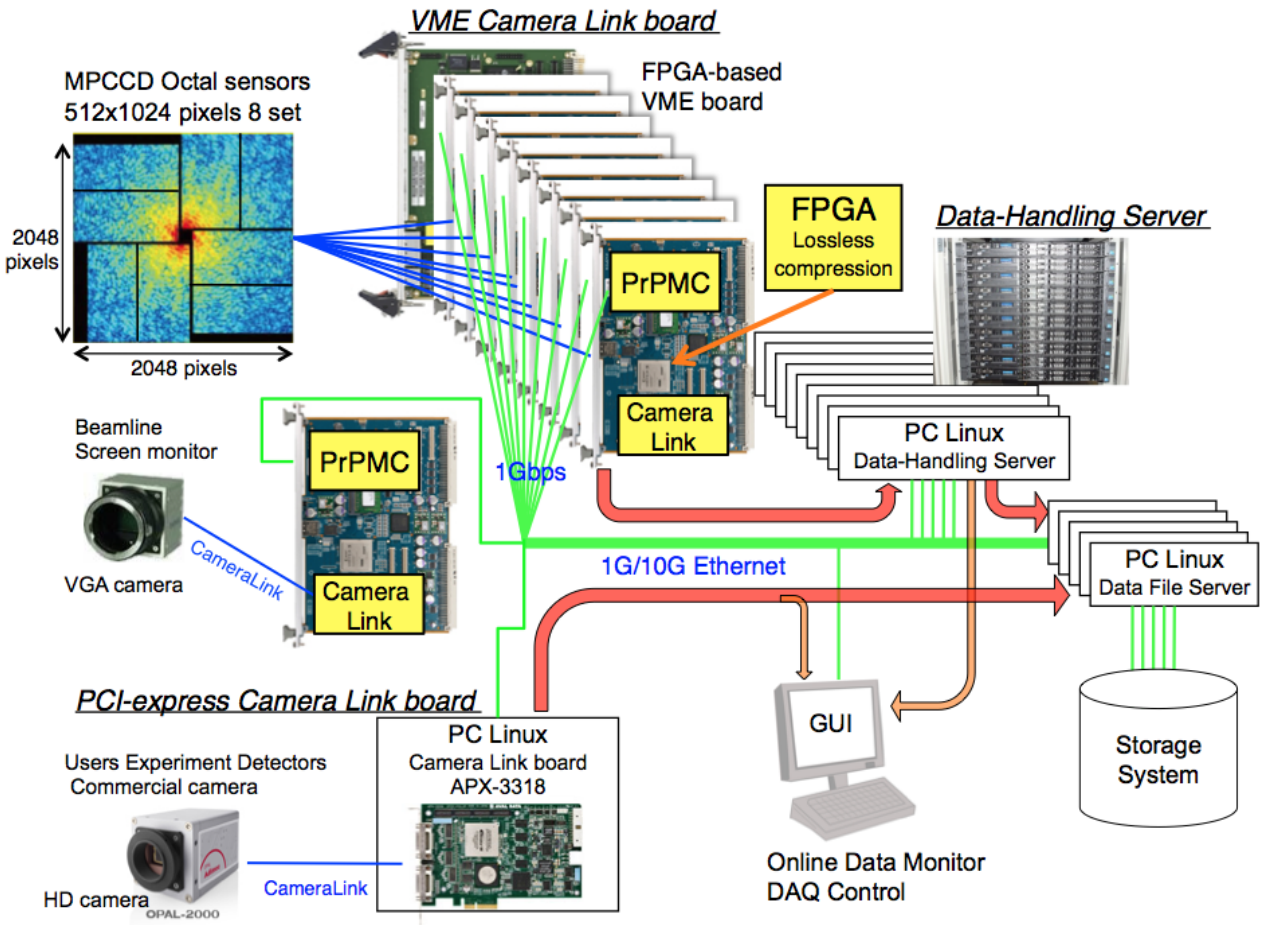

Figure 2: Schematic view and data flow of the image data-acquisition system (VME and PC).

Off-the-Shelf PCI-Express Camera Link Board

The PCI express Camera Link board (AVALDATA APX-3318) is employed on the operating system CentOS 5.4 for the sensor calibrations of MPCCD detectors. Long-term stability of the data transfer performance with this board in conjunction with high-definition (1920x1080 pixel) CCD cameras (Adimec OPAL 2000) has been successfully examined under the SACLA DAQ system. The stability verification with scientific CMOS camera (pco.edge PCO AG, 2560x2160 pixel) is now in progress. The current status of the VME-based and the PC-based Camera Link data acquisition are summarized in Table 1.

DATA-HANDLING SERVER

Figure 2 shows the schematic view and data flow of the VME-based and the PC-based image data acquisition systems. The data-handling server receives the data from the VME Camera Link board by TCP/IP socket connection. Each sensor data is transferred to the corresponding data-handling server, and stored temporally to a ring buffer in the server memory after formatting the data structure. Another process on the data-handling server reads the data from the ring buffer and provides a TCP/IP data transport service. A client process on a data file server receives the data and writes them to the connected high speed storage comprising of StoreNext single file system on the DDN (Data Direct Network) S2A9900 Storage. Total data throughput with 12 MPCCD sensors reaches 5.8 Gbps was achieved without any loss of the data.

Table 1: Current Status of VME-based and PC-based Camera Link Data Acquisition

	VME system	PC system
No. of support cameras	2	>100
Supported Camera Link configuration	base only	Base, medium full
Camera clock	< 80MHz	< 85MHz
Loss-less compression	Yes	No
MADOCA control	Yes	Yes

Another server process on the data-handling server offers data transmission service to the on-line data monitors. The process can provide basic analysis features such as averaging, region-of-interest statistical analysis, line profile calculation etc. User can also implement their own analysis code on the data-handling server to monitor

their experimental conditions. All these client-server processes as well as the board configuration control processes are controlled by the MADOCA framework [4] in order to achieve rapid implementation in the distributed SACLA DAQ system.

BEAM COMMISSIONING

The electron beam commissioning at SACLA started in February 2011, and the first light was observed in March. After three months of beam tuning, the first X-ray laser was observed in June. In the course of the commissioning, the DAQ system has been employed extensively for X-monitoring the spontaneous X-ray from the undulators, and X-ray laser characteristics.

SUMMARY

The image data acquisition system has been developed for the X-ray 2D detector and optical cameras at SACLA. We have developed a VME Camera Link board. We demonstrated that the data transfer from the MPCCD detectors to the high-speed data storage at a transfer rate of 5.8 Gbps. The off-the-shelf PCI-express Camera Link board was also implemented in the system in order to support wider range of cameras.

ACKNOWLEDGEMENT

The authors would like to thank Mr. Yu Kirino, Mr. M. Nagasaki, Mr. Y. Yoshioka and other members of ARKUS Corporation for the development of VME Camera Link board.

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