TIMING SYSTEM OF THE TAIWAN PHOTON SOURCE

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Abstract

The timing system of the Taiwan Photon Source provides synchronization for electron gun, modulators of linac, pulse magnet power supplies, booster power supply ramp trigger, bucket addressing of storage ring, diagnostic equipments, beamline gating signal for top-up injection and the time-resolved experiments. The system is based on event distribution system that broadcasts the timing events over optic fiber network, and decodes and processes them at the timing event receivers. The system supports uplink functionality which will be used for the fast interlock system to distribute signals like beam dump and post-mortem trigger with less than 10 μsec response time. The hardware of event system is based on 6U CompactPCI (cPCI) form factor and available in 2011. Implementation of the software is preceding. Timing solutions for the TPS project will be summarized in the following paragraphs.

INTRODUCTION

The TPS is the latest generation synchrotron light source. Event based timing system is applied for TPS due to its high performance and flexibility which has been already verified in many advanced light sources [1]. The EVG/EVR modules for TPS project are available in December of 2010. Efforts to setup the test system were done in the first quarter of 2011. The prototype system had already applied for the TPS 150 MeV linear accelerator commissioning and acceptance during the second quarter of 2011 with highly success. Developing various software support for event system in on going. Preliminary testing of TPS timing system is on going [2]. All development will be finished before the installation of the whole event system which is scheduled in 2013.

INFRASTURCTURE

The TPS timing system is an event based system. A central event generator (EVG) generates events from an internal sequencer and external sources [3]. These events are distributed over optic fiber links to multiple event receivers (EVRs) [4]. The EVRs, which are located in the control system interface layer, decode the events referred to as hardware triggers or software interrupts. For the linac, the decoded events are further encoded by a gun transmitter and sent over a fiber link to the gun high voltage platform. The external event sources include PPS signal which is locked to GPS, AC mains 60 Hz trigger, post-mortem trigger after beam loss and machine protection system trip. The event clock is derived from the 499.654 MHz master oscillator so that it is locked to change in the RF frequency. Fig. 1 shows an overview of complete TPS timing system and interconnections between its basic components. The master oscillator can be used as an external reference from a GPS disciplined Rubidium 10 MHz clock. Fig. 2 shows TPS timing modules include EVG, EVR, EVRTG and linac gun trigger receiver. The major part of the event system is realized as a 6 U cPCI form factor to compliant control hardware standard for accelerator controls at Phase I.

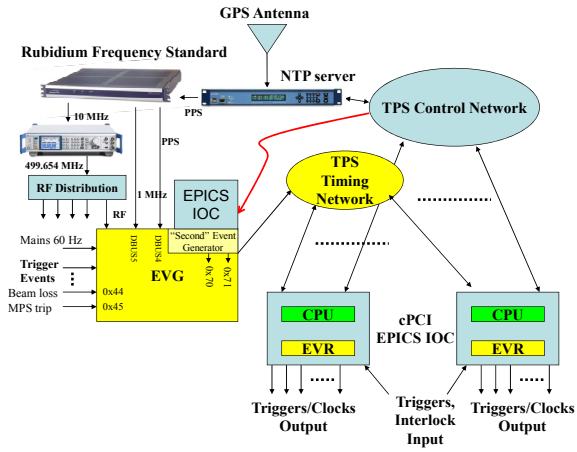

Figure 1: Block diagram of the TPS event system.

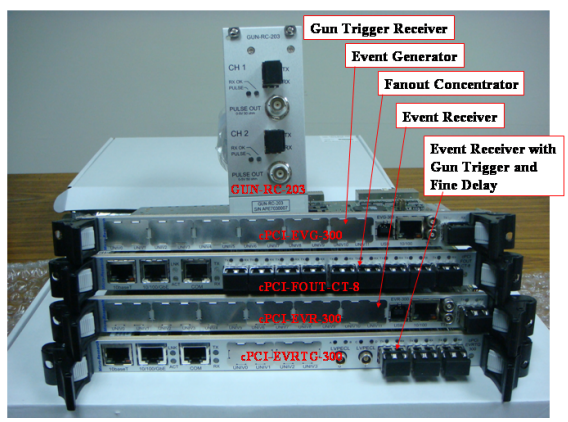

Figure 2: TPS timing modules.

Event Generator

The cPCI-EVG-300 generates event frames consisting of an 8-bit event code and an 8-bit distributed data bus, at a rate of 125 MEvents/sec. Events can originate from external trigger events, sequence RAM, software events and events received from an upstream event generator. Events from different sources have different priorities which are resolved in a priority encoder. A block of RAM is used to store a sequence of events. In cPCI-EVG-300 the input RF clock (499.654 MHz) is divided by 4 to

generate the event clock for the TPS timing system. Therefore, the resolution of timing event is 8 ns.

Event Receiver

The cPCI-EVR-300 and the cPCI-EVRTG-300 are the current available versions of 6U cPCI EVR. The cPCI-EVR-300 recovers the event stream and splits the event frame into the 8-bit event code and the 8-bit distributed data bus. The decoded events are mapped through RAM on to: trigger twelve pulse generators with programmable delay and width (32-bit prescaler from the event clock, 32-bit delay and 32-bit width) or set/reset twelve pulse generators. This EVR provides 3 programmable 16 bit prescaler from the event clock. Six UNIV I/O slots provide twelve front panel outputs can be mapped to any output such as each pulse generator output, prescaler and distributed bus bit. The cPCI-EVRTG-300 has eight channels; it includes two UNIV I/O slots support up to four various output and input, two LVPECL outputs and two SFP outputs. It is embedded jitter cleaner to deliver low jitter functionality of the EVR.

E-Gun Driver

The cPCI-EVRTG-300 has two SFP ports that can generate modulated optical signals that can be decoded by the GUN-RC-203 for linac gun driver trigger. The two SFP ports share an external inhibit signal. The GUN-RC-203 consists of two channels to provide single-bunch and multi-bunch injection respectively. It is realized as a cPCI-EVRTG-300 in the linac timing crate and a GUN-RC-203 placed on the gun HV platform. The fine programmable delay is also available and allowed to adjust the triggering position with a resolution of 10 ps over a range of 10 ns. The GUN-TX-203 mode has been designed to operate output pulse delayed by 1/4, 2/4 and 3/4 event clock period (~2, 4, 6 ns). The new module GUN-RC-300 will support arbitrary pattern generation functionality.

TIMING DISTRIBUTION

The distribution of the event stream will be a fiber optics with tree structure combined with single mode fiber (SMF) as well as multi-mode fiber (MMF) from cost points of view. The long distance link from the timing master to equipments area (Control Instruments Area, CIA, total 24 CIAs around the TPS storage ring and booster synchrotron) will be by SMF, while in CIA to EVR module will be OM3 MMF. Based upon experiences of several running light source, there will several tens of picoseconds drift in the year around due to ambient temperature change of the fiber distribution route. Several tens of picoseconds long-term drift might not cause a problem for most of applications. Drift compensation scheme by sensing fiber which lay around the facility was proposed to measure the long-term drift and make compensation globally. However, this might a correct that the timing fiber link route different path, which might have different environment, the global compensation cannot eliminate the drift for all links. Compensation for each link is standard approach for the RF reference distribution but not for event system yet. To deal with some timing station which need small time drift, the fiber link can replace the phase stabilized optical fiber (PSOF), and PSOF has a propagation delay temperature coefficient roughly 15 times better than standard optical fibers. The scheme of the fiber cabling is still in planning phase. The fiber cabling scheme will be decided in 2012.

TIMESTAMP

The Event System provides a global timebase to attach timestamps to collected data and performed actions. The time stamping system consists of a 32-bit timestamp event counter and a 32-bit second counter.

The timestamp clock and timestamp reset clock are assumed to be raising edge aligned. In the EVG the timestamp reset clock is sampled with the falling edge of the timestamp clock. In the EVR the reset is synchronized with the timestamp clock.

The two seconds counter events are used to shift in a 32-bit second value between every timestamp reset events. In the EVR the value of the seconds shift register is transferred to the seconds counter at the same time the higher running part of the timestamp counter is reset.

The distributed bus event inputs of EVG can transmit timestamp clock and timestamp reset clock independently through the distributed bus event enable register.

EVG will automatically increment and send out two seconds counter events. Using this feature requires the two externally clocks, and the events 0x70 and 0x71 get generated automatically. The timestamp generation of EVG is shown in Fig. 3.

After the rising edge of 1 PPS on DBUS4, the internal seconds counter is incremented and the 32 bit binary value is sent out LSB first as 32 events 0x70 and 0x71. Host CPU can acquire UTC second from NTP server and set second register, load to second counter and enable timestamp generator by on-demand (system boot, cold start).

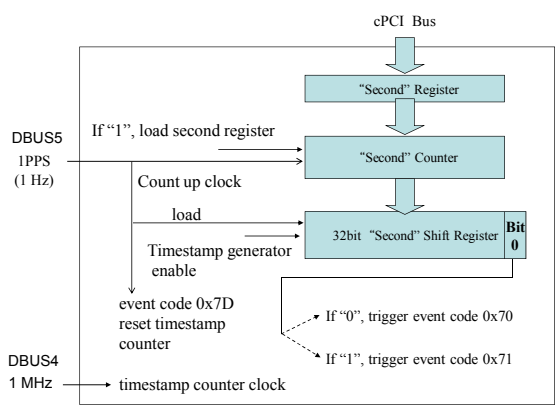

Figure 3: Timestamp generation at EVG.

The timestamp event counter either counts received timestamp counter clock events or runs freely with a clock derived from the event clock. The event counter is

also able to run on a clock provided on a distributed bus bit. The timestamp event counter is cleared at the next event counter rising clock edge after receiving a timestamp counter reset event. The seconds counter is updated serially by loading zeros and ones into a shift register MSB first. The seconds register is updated from the shift register at the same time the timestamp event counter is reset. Fig. 4 shows block diagram of timestamp logic at EVR.

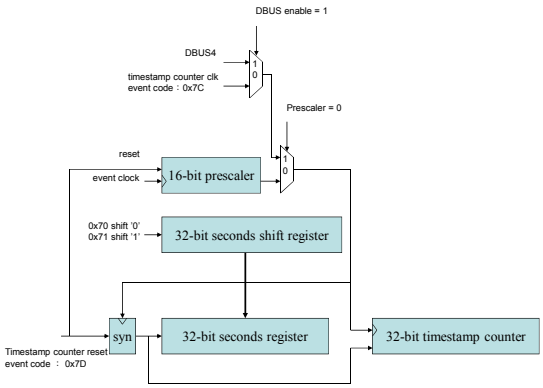

Figure 4: Timestamp logic at EVR.

TIMING SYSTEM DIAGNOSTICS

In normal operation, the rising edges of booster clock, storage ring clock and coincide clock should be lock. Machine clocks are monitored using an oscilloscope. EPICS support for the oscilloscope is prepared. Simple pattern analysis software (Matlab scripts) will analyze the relationship of clocks. If clocks out of lock, it will alarm and stop the system. A time to digital converter (TDC) measure timing difference amount clocks is another auxiliary supports. The wiring schematic is given in Fig. 5. The TDC module will analyze the positions of the clock edges and measures the mismatch. The oscilloscope will display machine clocks waveform for operation. If the machine clock mismatch exceeds 10 ns, then a SYN-FAIL signal will be sent to the machine protection system and notify operators.

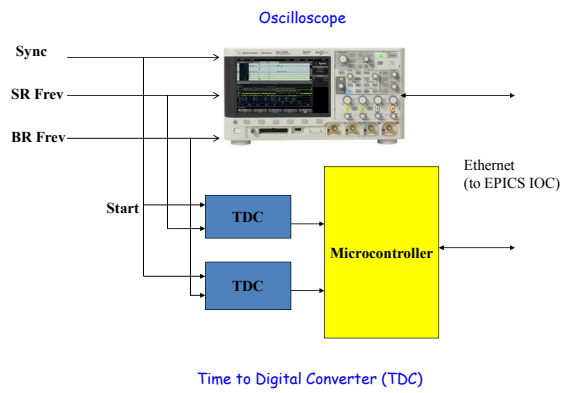

Figure 5: Timing system healthy monitoring.

Based upon the reports of several light sources, there are several tens of psec drift around the year. This is acceptable for most of the accelerators timing and users timing requirement. However, to measure the timing drift of specific links, several approaches can be used.

1. Measure the RF clock versus machine clock edge at EVR site. It needs a stable RF reference available at site.
2. Measured an environment sense fiber around the ring back to the timing master. The difficult is that each link might expose different route on the cable tray. There are some local heating sources on the tray due to the nearby power cables.

TIMING INTERFACE FOR BEAMLINE

The timing interface was developed to provide hardware signals for synchronization of beamline equipment with the electron bunch structure in the storage ring and with the process of Top-up operation. Signals at each experiment station include RF clock, machine clock, top-up injection gating. Top-up gating signals include long gate over whole top up injection cycle and short gate over top up for single injection cycle and few unassigned channels that can be configured to user requirements. For the beamline need high precision timing to synchronize their laser system or data acquisition system, sub-ps RF link will be available.

CONFIGURATION TOOLS

The timing system is integrated into the TPS EPICS control environment. The EVG configuration pages define the options of cPCI-EVG-300. These include configuration of the EVG operating mode, selection of RF and AC divider, definition of multiplexed counter, optional transmission of software events, enable of event trigger inputs and specify event code and timestamp into the sequence RAMs. The EVR configuration pages configure the options for the cPCI-EVR-300, such as pulse delay, width and polarity, front panel output assignments and distributed bus enable and event decoding mapping RAMs. Applications to control the timing system are built with the usual EPICS tools for databases and EDM for user interface.

DOWNLINK AND UPLINK FUNCTIONALITY

The event system not only distributes events to EVRs but also deliver event uplink functionality by the help of the fanout concentrator.

Measurement of the global response time for the TPS timing systems uplink and downlink is presented in Fig. 6 for two stage fanout concentrator and 310 m single mode fiber. This event code 0x45 is used for indication of MPS-TRIP event. The event is stimulated by an external trigger produced by an EVR2. According to the oscilloscope pattern the EVR2 transmitted event by MPS-TRIP trigger and EVR1 decoded event pulse are shifted with respect to each other by 2.45 μs. The global response time is 4.42 μs which consists of EVG, EVR1, EVR2, three fan-out

concentrators processing times and propagation delay time along timing system fiber network (Fig. 6).

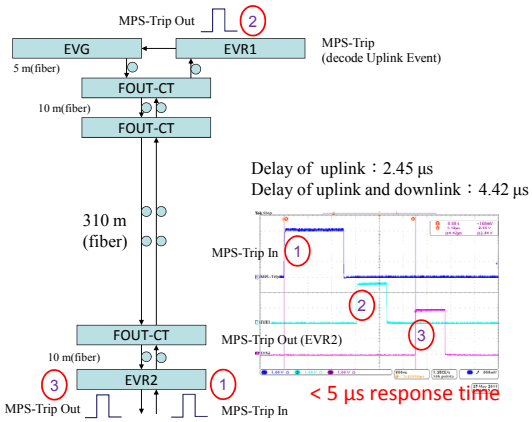

Figure 6: Timing measurement of uplink and downlink with 310 m fiber and three stages of fan-out concentrator.

INJECTION SEQUENCE CONTROL

To accommodate various operation and injection scenarios of the TPS storage ring and booster synchrotron, sequence control plays a crucial role. The sequence is stored at sequence RAM of the EVG module. Adopting Matlab scripting for the sequence control of the TPS accelerator is considered seriously due to expertise of available manpower and high productivities compare to another tools. The timing sequence control is also considered to use Matlab scripts embedded in the timing master EPICS IOC which host the event generator module. Since the TPS machine repetitive rate is 3 Hz, the booster power supply ramping waveform is 3 Hz sinusoidal wave and T-ZERO defined at 0 msec. The storage ring extraction time is T-ZERO+166.66 msec. There are sufficient time for sequence RAM management (start/stop, replace contents of sequence RAM locations …etc.). The scripts will access (read and set) the EVG related EPICS PVs by LabCA. So, the sequence control OPI can set parameters related to the sequence and execute by the sequence control scripts running in the timing master EPICS IOC.

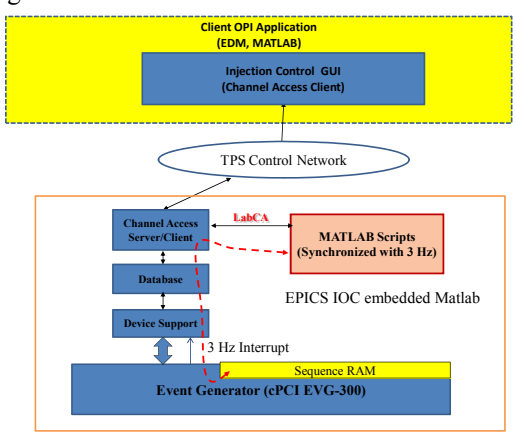

Figure 7: Block diagram of proposed timing sequence control.

The Matlab scripts for injection sequence control detect sequence RAM interrupt, check injection conditions or operation modes and replaces sequence RAM contents. The Block diagram of timing sequence control is represented in Fig. 7. All parameters for the machine operation modes and parameters will be designed as specific EPICS PV, such as bucket address, repeat cycle, top-up injection, decay mode and etc. Preliminary operation modes supported includes:

a. E-gun pulser: multi-bunch and single bunch.
b. Multi-bunch width adjust.
c. Booster magnet cycle before beam trigger.
d. Storage ring septum cycle before beam kicker fired.
e. Next injection bucket address.
f. Top-up-mode injection.
g. Fill pattern management.
h. Inject to target current.
i. Individual element trigger for component test.
j. Booster + linac operation only.
k. Linac operation only.
l. Auto stop injection when safety interlock actuated, stored current exceeds target value.
m. …etc.

SUMMARY

The event system for the TPS project is being implementation stage. The prototype has been deployed in early 2011 for linac acceptance test. Configuration tools have been developed and revised continually. Preliminary sequence control is in proceeding. Timestamp function of event system will be tested.

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