NETWORK ON CHIP MASTER CONTROL BOARD FOR NEUTRON ACQUISITION

E. Ruiz-Martinez*, T. Mary, P. Mutti, J. Ratel and F. Rey. Institut Laue-Langevin, Grenoble, France

Abstract

The acquisition master control board is designed to assemble the various acquisition modes in use at the Institut Laue-Langevin (ILL). The main goal is to make the card common for all the ILL's instruments in a simple, modular and open way, giving the possibility to add new functionalities in order to follow the evolving demand. It has been necessary to define a central element to provide synchronization to the rest of the units. The backbone of the proposed acquisition control system is the denominated master acquisition board. The master board consists on a VME64X configurable high density I/O connection carrier board based on the latest Xilinx Virtex-6T FPGA. The internal architecture of the FPGA is designed as a Network on Chip (NoC) approach. The complete system also includes a display board and *n* histogram modules for live display of the data from the detectors.

INTRODUCTION

The master board centralizes the timing information and the synchronization signals used in the hardware management of the data acquisition of the instrument. At the ILL the standard acquisition system common to most of the instruments is based on a VME bus solution, where all the boards become slaves of one master card.

The present article reports on the development of a master board using a general-purpose carrier card for use in future applications. The MPC 1200 carrier board has been developed by collaboration between IOxOS Technologies and the Instrument Control Service (SCI) at the ILL. The document will start with the description of the network on chip approach using a Virtex 6 FPGA. The MPC 1200 carrier board section describes the multiple features, the IO connections and the devices present on the board. The MPC front-end section summarizes the MPF modules used in the carrier board and the design of the front panel used within the master acquisition application. The implementation part explains the main blocks employed in the master acquisition and the development kit provided in the TOSCA II architecture. The discussion will end with the main conclusions gathered in the development of the project.

NETWORK ON CHIP

The standard shared bus architecture, widely used since years, is all based on master/slave interactions. A master reads or writes one or several slave resources, which can be IO registers and/or memory locations. Several new trends have been introduced like for instance cache memory, optimized burst transactions, split transactions with un-compelled request and completion, but without modifying fundamentally the initial principle. These standard shared buses have two main inconvenient:

- the physical media interconnecting the masters with the slaves shall be shared. In order to allocate the media to the master an arbitration mechanism is needed with a direct impact on the latency and the bandwidth performance.
- the physical media size (number of pins) is limited in construction. It is difficult to built interfaces with thousands of IO.

The TOSCA II architecture has been defined to support the shared bus architecture but with optimal latency and bandwidth performance. The implementation has been done in new high performance Xilinx Virtex-6T FPGA. The interconnection between the masters and the slaves are no more implemented with a shared media but with a full mesh switch where the master owns a direct connection to every slave. This approach presents the following advantages.

- due to point to point connection the bandwidth performance is not shared and can be specifically defined by the master and the slave implementation.
- due to individual connection between masters and slaves, the latency is fully under the control of the slave and no more related to the media sharing.

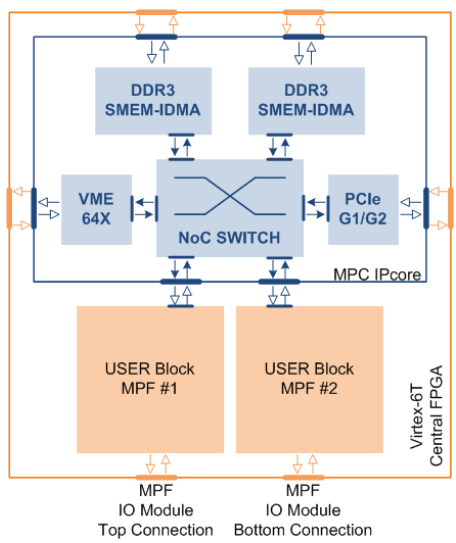

Figure 1: Network on chip architecture.

The NoC approach, see Figure 1, is possible thanks to the fact that the targeted FPGA has enough resources (DPRAM and LE) and that there is no limitation in the number of connections inside the FPGA routing. Another key feature of the TOSCA II Architecture is based on the

*ruizmartinez@ill.fr

full availability of the interface IP core, at VHDL source level for all the key functions (PCI, PCI Express, DDR2/DDR3 controllers, DMA engines, switch infrastructure) [1].

The XILINX Virtex-6T Central FPGA top is organized in a hierarchy level composed of two main blocks:

- the MPC IP core integrating the basic carrier board infrastructure as NoC switch, PCI express EP, VME64x master/slave, the DDR3 shared memories controller with IDMA and the interrupt controller
- two USER blocks, one for each MPF IO connector, fully configurable by the end user.

The MPC IP Core is released in binary format (NGC), along with generic USER block examples and the needed files for the implementation of a fully functional FPGA for the MPC 1200.

MPC 1200 CARRIER BOARD

Compared to other products based on mezzanine cards extension (i.e., FMC or XMC), the MPC 1200 edge-to-edge interconnection solution, see Figure 2, provides full PCB area utilization, direct VME64x front panel access without any restriction on front panel connectors type, and enhanced air cooling capability with standard heat-sink while keeping modularity and versatility.

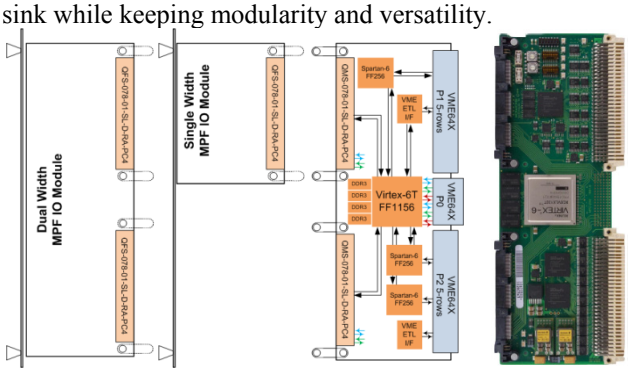

Figure 2: MPC 1200.

The central Virtex-6T FPGA embeds a proprietary IP core providing a complete master/slave VME64x interface. The master/slave VME64x IP core is part of the TOSCA II infrastructure and therefore provides transparent bridging capability such as PCI Express to VME64x [2].

The VME slave interface implements the legacy VME/VME64 addressing configuration with static switches and/or VME64x CR/CSR. The VME slave handles all addressing modes and is fully programmable through an in-going scatter-gather. The VME master interface, driven by the internal FPGA infrastructure supports also all VME addressing mode including 2eVME and 2eSST.

The MPC 1200 integrates on-board DC-DC power supplies for the on-board FPGA and for the MPF IO modules. These DC-DC power supplies are also dimensioned to support the whole Virtex-6T device family. To fully support the Virtex-6T Central FPGA capability, the MPC 1200 integrates three additional Spartan-6 XC6SLX9- FF256 companion devices. Two are dedicated to the VME P2 User IO support and the third one is used for power-up management and FPGA configuration.

The VME P2 user IO (32+32+40 signals on 5-rows connector, see Figure 3) is supported through the two Spartan-6 programmable routing infrastructure providing a 5 V tolerant electrical interface with the P2 connector. The interconnection with the central Virtex-6T FPGA is supported through high-speed (up to 1Gb/s) low level 1.8 V SE or DE signaling.

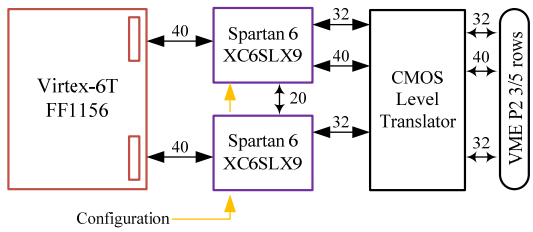

Figure 3: VME64x P2 User IO.

The master acquisition board uses the VME P2 signals to manage the synchronization among the different acquisition and histogram modules. These signals are shared with the boards present in the crate. The input/output direction of the P2 signals is configurable depending on the instrument mode of acquisition.

The FPGA configuration is assured by power on (PON) finite states machine (FSM) implemented in a Spartan-6. The FPGA configuration bit-streams for the Spartan-6 and Virtex-6T are all stored in high-speed serial flash EPROM devices. The FPGA bit-streams can be directly downloaded from the VME slave interface or PCI Express EP.

The carrier board includes as well four 128 Mbit SPI Flash EPROM devices with 4-bit read-out. Four DDR3 memory devices are connected to the Virtex-6T central FPGA. These memory devices can be interfaced as two or four independent DDR3 controller. The DDR3 memory controller IP core provides the complete control of the DDR3 devices and it has been fully integrated in TOSCA II. Other functions such as I2C and SPI interfaces, GPIO management, PON FSM controller, and power supplies monitoring, are integrated within the Virtex-6T central FPGA firmware.

MPF FRONT END

Two Multi-Purpose Front IO (MPF IO) module sizes are supported. The single-width size is derived from the 3U eurocard and the dual-width from the 6U eurocard.

The MPF IO Modules solution has several advantages compared to the FMC extension approach:

- larger PCB size available
- direct access to the front panel without limitation on the IO connectors (no micro connectors required).

- full VME component height allowing installation of heat-sink on critical devices.
- better physical and galvanic isolation for noise sensitive application (i.e. ADC with resolution better then 12-bit).

The MPF IO modules are attached to the MPC 1200 carrier through the SAMTEC QFS/QMS connectors (see Figure 4). The MPC 1200 provides to the MPF modules a full collection of power supplies with up to 4.1 A. (8.2 A on the 1.0 V). For each MPF connector the Virtex-6T IO support is limited to 100 SE (50 DE) signals distributed over 2.5V Virtex-6T IO banks. The use of Spartan-6 devices as data concentrators boosts data bandwidth up to 50 Gb/s [2].

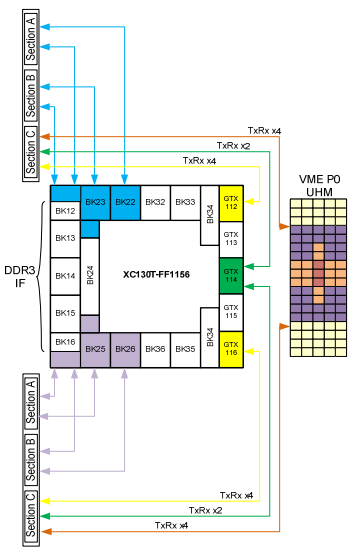

Figure 4: Front panel MPF IO connection.

The front end of the master acquisition board contains the signals coming from external modules involved in the acquisition procedure, like pulses from a rotating machine or an external clock for synchronization purposes. These signals have been grouped in a customized front panel with 12 one-point LEMO for individual inputs, and a DB26 high-density connector. In future applications the front panel could be modified including a processor, flash ADC digitizers or high speed digital connectors for high performance applications [3].

IMPLEMENTATION

The implementation of the master acquisition board has been developed in VHDL using the user area of the TOSCA II architecture. TOSCA II is delivered with full VHDL source code together with a set of test-benches and bus functional models (BFM) to set up a complete VHDL simulation environment for functional verification purposes. The TOSCA II architecture is based on a PCI Express switch centric structure implementing a memory mapped model with segregated I/O space (control plane) and memory space (data plane) [4].

In the master acquisition board each acquisition mode in use at the ILL is developed in a functional and independent block. These blocks are able to manage the synchronization signals, using the front-end and the VME P2 interface, according to the specific needs of the instrument. Depending on the measurement technique adopted, the following acquisition modes are accessible via the master board [5]:

- Simple integral count: available for both single and multi-detectors, it allows a neutron's counting time from 100 *ns* to $(2^{64}\text{-}1)\cdot 10^{8}$ *s* with a time resolution of 100 *ns*. While the gate generated by the master acquisition board remains active all the neutrons arriving at the detector will be counted and the corresponding histograms are stored in the acquisition cards.
- Time of Flight (ToF): the continuous neutron flux produced by the ILL's reactor is pulsed by means of a rotating chopper with frequencies between a few Hz up to 500 Hz. The energy of a detected neutron is calculated starting from the traveling time from the chopper to the detector once the distance of the two elements is known. The master acquisition board is able to manage four independent ToF consisting of up to 2048 variable duration time channels, from 100 *ns* up to 43 *s*. The acquisition card will provide the corresponding histograms where all the detected neutrons are arranged as a function of their arrival time.
- Kinetic: used especially for soft matter studies to trace phenomena with long duration in time, it is very similar to the previous mode. In this case the neutron flux is continuous and the start signal is delivered by an external event. The acquisition card delivers time-slice histograms where the neutrons are arranged according to their arrival time. A combination of ToF and Kinetic mode is also possible when a chopper is available on the instrument. In this case the neutrons in each kinetic time-slice are arranged according to their respective ToF.
- Doppler: two backscattering spectrometers are equipped with a Doppler motion at the monochromator. This last one is moved with a velocity parallel to the reciprocal lattice vector [6] and, as a consequence, the energy of the reflected neutron is modified via a longitudinal Doppler effect. The velocity of the monochromator is varied periodically following a sinusoidal function. The master acquisition board receives via the front-end external synchronization signals corresponding to different velocities. The acquisition card produces a histogram where the neutrons are accumulated into the corresponding equidistant velocity channels.
- Oscillating Radial Collimator (ROC): diffraction experiments on instruments equipped with Position Sensitive Detectors (PSD) suffer from background originated by the sample environment [7]. A specific diffracted beam collimator has been designed to reduce the off-sample parasitic scattering without

perturbing the resolution or the scattering from the sample. This collimator is oscillated through a specific angle with a linear angular velocity. The master acquisition board coordinates the neutron's count depending on the movement of the collimator.

CONCLUSION

As shown in the previous section, the instruments at the Institut Laue-Langevin required a large variety of acquisition modes. This, together with the need of properly synchronize several acquisition cards, has pushed the development of a new master acquisition board. An inappropriate management of all the different external signals connected to the acquisition could cause loses of information during the experiment and/or in the subsequent data analysis. Versatility is a mandatory requisite for the new board since it should be adapted to all the instruments without major changes. The results of all those constraints is a master board design conceived as a VME carrier board with high density I/O connection, leaving the autonomy to use the front-end for custom applications. The board is based on a central Virtex-6 FPGA which embeds a full mesh switch where the master owns a direct connection to every slave, having fully connection with the resources present in the board: PCI express, VME64X master/slave, DDR3 memory controllers and the user area, where the master acquisition application has been implemented.

REFERENCES

[1] J. Bovier, "MPC 1200 Hardware-Software Interface Data", IOXOS technologies internal report, (2009).
[2] J. Bovier, "MPC 1200 – Multi-Purpose IO Carrier VME64X IO Interface", IOXOS technologies, (2011); http://www.ioxos.ch.
[3] T. Mary, F. Rey, J. Ratel, "New acquisition system", Institut Laue-Langevin internal report, (2011).
[4] J. Bovier, "MPC 1200/ IFC 1210 TOSCA II Simple USER Block", IOXOS technologies internal report, (2011).
[5] J. Ratel, "Interface VME Master Acquisition", Institut Laue-Langevin internal report, (2011).
[6] B. Frick, "Neutron and X-Ray Spectroscopy", Part 2, p. 483 (2006).
[7] J. Bouillot and J. Torregrossa, Revue Appl. Phys. 19 (1984).