ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-THMPL09

VME BASED DIGITIZERS FOR WAVEFORM MONITORING SYSTEM OF LINEAR INDUCTION ACCELERATOR LIA 20

E. S. Kotov†,[1], A.M. Batrakov, G.A. Fatkin[1], A.V. Pavlenko[1], K.S. Shtro, M.Yu. Vasilyev[1],
Budker Institute of Nuclear Physics, Novosibirsk, Russia
[1]also at Novosibirsk State University, Novosibirsk, Russia

Abstract

Waveform monitoring system plays a special role in the control system of powerful pulse installations providing the most complete information about the installation functioning and its parameters. The report describes the family of VME modules used in the waveform monitoring system of a linear induction accelerator LIA-20. In order to organize inter-module synchronization the VME-64 bus extension implemented in the VME64-BINP crates is applied in the waveform digitizers.

INTRODUCTION

Waveform monitoring system (WMS) includes "fast" and "slow" monitoring subsystems. To obtain the necessary waveforms with different duration, a several fast and slow models were developed. The models use unified hardware solutions in the interface part interacting with the VME bus. The interface part of the modules performs not only VME-bus standard procedures but also provides interface with additional synchronization lines that are present on the J2/P2 connector [1]. With these lines, the phased-clocking of analog-to-digital converters is provided for all digitizers in the crate.

Three types of digitizers are involved in “fast” subsystem. The first one, ADC4x250-4CH, is 4-channel 250 MSPS digitizer. The second one, ADC4x250-1CH, is single channel digitizer with sample rate of 1 GSPS. The third model intended for operations with signals in optical diagnostics which require bandwidth about 100 MHz and sample rate 250 MSPS. Resolution of devices is 12 bit. All of fast models are based on unified hardware platform and differ in timing as well as the structure and schematics of the input amplifiers.

"Slow" subsystem is based on ADCx32. This digitizer uses four 8-channel multiplexed SAR ADCs (1 μs conversion cycle) with 12 bit resolution. The total number of channels of ADCx32 is 32. Main feature of this module is program configurable channel sequencing which allows to measure signals with different duration.

FAST DIGITIZERS FAMILY ADC4X250

The most used model ADC4x250-4CH intended to record accelerating voltage waveforms. The total number of such signals reaches 840. These data allow us to determine the beam energy and monitor the correct operation of the high-voltage modulator.

The fastest model ADC4x250-1CH allows monitoring the voltage in kickers – the beam deflecting devices. The total number of these signals is about 10.

The third digitizer processes signals coming through optical lines and contains a photodetector at the input.

Unified Hardware Platform

A relatively small number of kicker signals makes uneconomical the development of the device with 1 GSPS sample rate if take into account labour expenditures. On the other hand, the purchase of a number of modules, each of which costs about $12,000, not a satisfactory one. However, it is clear that the structural schemes of all fast modules are very similar. In this regard, it looks attractive variant when all modules are designed as two separate PCBs that stacked with each other by mezzanine way. One PCB is unified mainboard shared by all fast digitizers. Its structural scheme is shown in Fig. 1. Sampling is performed by four 250 MSPS 12 bit analog-to-digital converters. Raw ADC data is stored into two SRAM chips with total capacity of 3 megasamples. Two FPGA Altera Cyclone III transfer samples from ADC to SRAM in the measure phase as well as applying calibration correction on-the-fly to reading out data. Furthermore, FPGA software performs common control functions and VME communication. Also board contains outstanding clocking chip for accurate ADC timing and synchronization.

Any device in family is obtained by connecting according preamplifier. Software of the module determines what kind of preamplifier is connected and then configure ADCs’ clocking scheme and internal registers in the correct way.

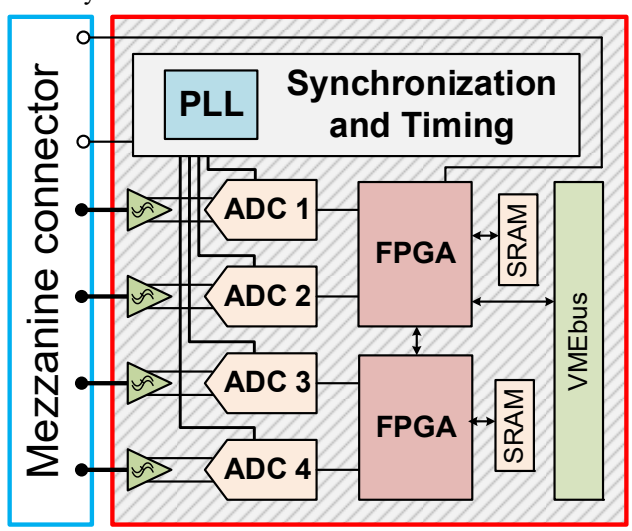

Figure 1: The structure of ADC4x250 mainboard.

† e.s.kotov@inp.nsk.su

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-THMPL09

ADC4x250-4CH

Mezzanine board preamplifier in the ADC4x250-4CH contains four identical channels. The signal from each channel is processed by its "own" ADC. The ADC-chips are clocked simultaneously therefore the sample rate of this device coincides with the sample rate of one ADC and equals 250 MSPS. The bandwidth of the ADC4x250-4CH is determined by the input amplifiers and equals 75 MHz. Also preamplifier contains precision DAC for periodically offset and gain calibration of each channel. The view of 4-channel model with installed amplifier is presented in Fig. 2.

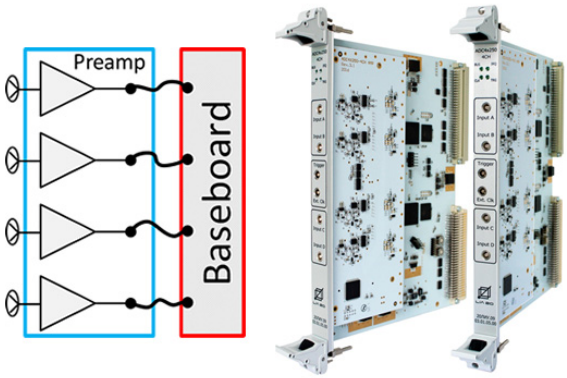

Figure 2: ADC4x250-4CH.

ADC4x250-1CH

One-channel device is obtained by program reconfiguration of a clock circuit and installing the 1-channel input amplifier, which has 300 MHz bandwidth. In order to achieve an effective sampling rate of 1 GSPS it is necessary to clock the ADC-chips in series one by one and with a phase shift of 90° (see Fig. 3). The difference in hardware latency in ADC timing, which is ±40 ps, is corrected programmatically using a special algorithms.

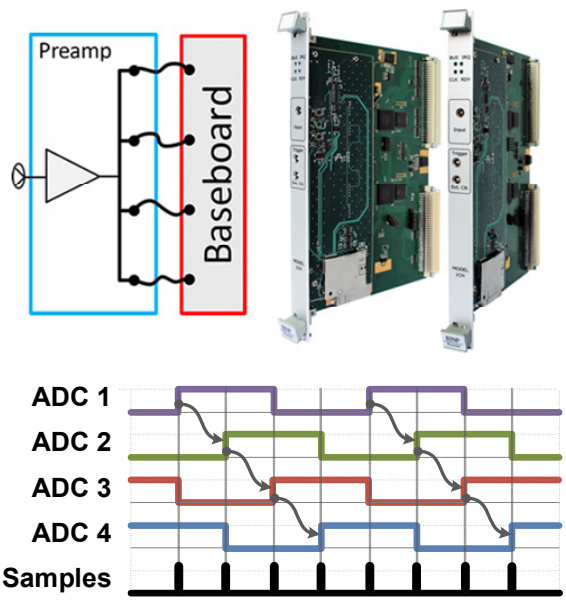

Figure 3: ADC4x250-1CH and its clock sequence.

ADC4x250-APD

Avalanch photodiode (APD) version designed as four-channel module with optical input. Photodiode using requires slightly different solutions in front-end but this challenge gracefully fit with unified hardware platform concept. In this case, preamplifier consists of avalanch photodiode with transimpedance amplifier for each channel (Fig. 4). Timing scheme of ADCs remains as in the -4CH device case.

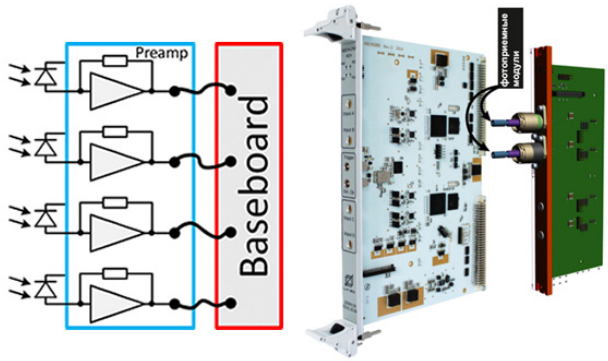

Figure 4: ADC4x250-APD.

Specification of the ADC4x250 family you can see in Table 1.

Table 1: ADC4x250 Family Specifications

	ADC4x250 -4CH	**ADC4x250 -1CH**	**ADC4x250 -APD**
Sample rate	250 MSPS	1000 MSPS	250 MSPS
Bandwidth, -3dB	75 MHz	300 MHz	120 MHz
Number of channels	4	1	4
Input ranges	±0.5 V, ±1 V, ±2 V, ±4 V		10 kΩ (86 μA_{max}) 40 kΩ (21 μA_{max})
Resolution	12 bit		
Buffer length	786 432 samples/ch	3 145 728 samples/ch	786 432 samples/ch
SNR in the BW	62.7 dB_{FS}	62 dB_{FS}	57.2 dB_{FS} @ 10 kΩ 47.7 dB_{FS} @ 40 kΩ

SLOW DIGITIZER ADCX32

"Slow" WMS subsystem provides data acquisition of Pulsed HV System (PHVS) signals. PHVS includes 27 HV chargers, 480 pulse modulators with Pulse Forming Networks (PFN) for supplying accelerating inductors, 64 pulsed demagnetizer and 32 magnetic lens power supplies. The durations of PHVS elements processes differ significantly as shown in timing diagram of PHVS opera-

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-THMPL09

tion (see Fig. 5). Thus, "slow" WMS should be able to digitize 1563 signals in time range 500 µs – 20 ms.

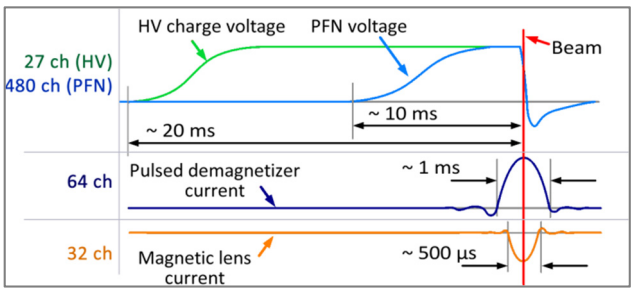

Figure 5: PHVS timing diagram.

The basic idea of "slow" WMS digitizer design is using four 8-channel multiplexed 1 MSPS SAR ADCs with programmable channel sequencing. Channel sequence configuration determines sampling rate for each ADC channel individually. That allows sampling channels with shorter time duration faster than channels with longer time duration. This approach is illustrated in Fig. 6. Sequence example is shown in timing diagram for the case, when CH0 of ADC records fast process with twice higher sampling rate than CH1 and CH2.

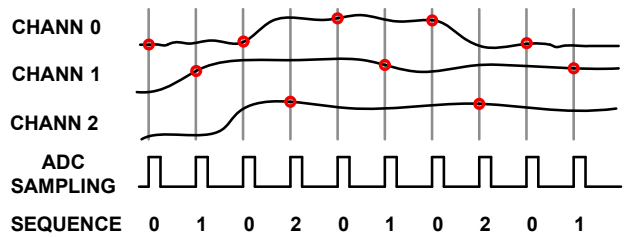

Figure 6: ADC channel sequencing.

ADCx32 block diagram is shown in Fig. 7. Digital part of the digitizer is based on Nios II embedded CPU implemented in a Cyclone III (Altera FPGA). Digital part provides VME interface support, driving of SDRAM memory, trigger and sample clock sources selection and analog front-end control. Front-end is built on four ADC chips and 32 input channels circuits. Digitizer inputs equipped with HV protection (100 V), 50 kHz filtering and PGAs. Photo of the module is presented in Fig. 8.

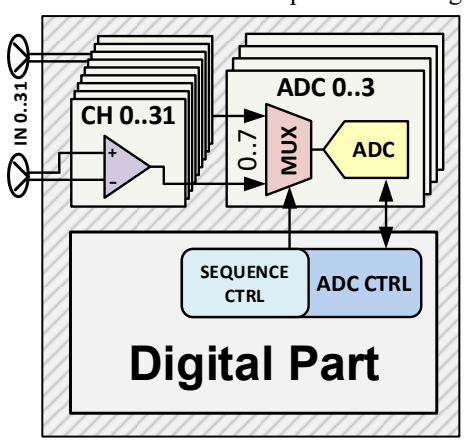

Figure 7: ADCx32 block diagram.

Necessary precision was achieved by using calibration procedure, which includes measurements of zero and scale errors of drivers and ADCs and applying built in data correction algorithm.

Specification of the ADCx32 is presented in Table 2.

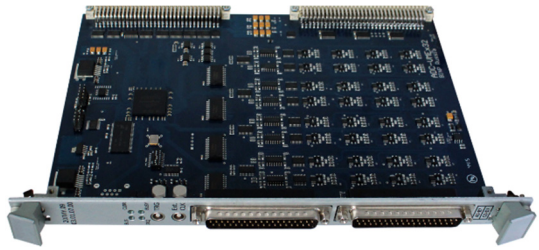

Figure 8: ADCx32 module photography.

Table 2: ADCx32 Specifications

Sampling rate	1 MSPS (max)
Bandwidth, -3dB	50 kHz
Number of channels	4 simultaneous
Total number of channels	8 x 4 = 32
Input ranges	±1 V, ±2 V, ±4 V, ±8 V
Resolution	12 bit
SNR in the BW	70.9 dB_{FS}
Buffer length	524 288 samples/ch

CONCLUSION

Four models of VME-based waveform digitizers, which intended for creating Waveform Monitoring System of the accelerator LIA-20 have been developed. Obviously, these modules can be successfully used in other VME-based systems to arrange multichannel recording of signals in wide time range.

The main feature of the described devices is the use of the inter-module synchronization signals, coming to connector J2/P2 from the additional lines of the lower VME databus. This feature allows to organize synchronous sampling procedures for all digitizers located in the crate.

Another feature of the work is the decision to develop and use a unified hardware platform for three models of fast digitizers. This solution significantly reduced the development stage.

At present, several batches of the described modules are manufactured in BINP experimental workshop and are in use in the control system of the LIA-20.

REFERENCES

[1] G. Fatkin *et al.*, "New VME-Based Hardware for Automation in BINP", ICALEPCS'2017, Barcelona, Spain, 2017, THMPL10, these proceedings