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NEW VME-BASED HARDWARE FOR AUTOMATION IN BINP

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Abstract

A new VME-based crate and modules are presented in this work. This hardware is primarily intended for LIA-20 control system, but we also plane to use it for the upgrade of the controls of existing complexes such as: VEPP-2000, VEPP-4, VEPP-5 Preinjector. Modules were designed with an ability to be used planned projects such as Super c-tau factory. A crate is 6U VME64x compatible crate with additional synchronization, daisy-chain lines and 6U RIO-modules. Each crate has a built-in status monitoring over CAN-BUS with independent power supply. A family of VME modules is based on the same design sample and include: digitizers, timing modules, CAN-interface module, interlock qmodule. All modules are cost effective and have TANGO device servers developed for them.

INTRODUCTION

Budker Institute has a long history of developing it's own electronic modules for automation. Most of the modules that are still used on current installations in the institute (VEPP4, VEPP2000, injection complex, GOL-3 and GDL), were developed in CAMAC format in 1970-1980-s. Now they are obviously morally and technically outdated. Considering more contemporary standards our group had some experience with using NI PXI, we developed a line of modules for magnetic measurements in VME standard [1] and we had automated LIA-2 accelerator [2] using in-house cPCI modules. We need a new modular standard for automation electornics both for our new projects such as LIA-20 [3], Super c-tau Factory, magnetic measuremetns, etc., and for upgrade of existing complexes.

When choosing the modular standart for automation we have to take into account our specific economical conditions and the experience of our electronics team. From our current point of view we could formulate a following set of requirements to the standard. First of all it should be a widespread modular standard with available COTS modules. Second, it should have lines for intermodule synchronization. Third, it should have rear input-output modules for convenient cabling. Fourth, to reduce the overall system cost a standard should allow as much modules in crate, as possible. And lastly we should consider our experience using and developing modules for it. The table 1 summarizes standards that we analyzed.

After considering these standards we found that there is no one fully satisfying our requirements. VXI is very expensive and has a small crate. CompactPCI has no synchronization lines and only 8 modules are supported. PXIe has no rear IO modules and though 6U crates are available standard ones are 3U. MicroTCA was found to be quite interesting, but it is excessively complex, not very widespread for automation and creating modules for it is an untrivial task. Our previous experience with VME was quite good, but it has no synchronization lines. Therefore we decided to create our modification of VME standard that will meet all our requirements. After the analyze we found out that there is CERN VME430 standard that is quite similar to what we have done though it uses 9U modules.

Table 1: The Analyze of Modular Stanards

Name	Synchr.	RIO	Modules	Exp.
VXI	+	-	13	±
VME	-	+	21	+
PXI(e)	+	-	18	∓
CompactPCI	-	+	8	+
microTCA	*	-	21	-

VME64-BINP CRATE

VME64-BINP is a 10U VME-64x compatible crate with 21 positions for 6U modules. The photograph of the crate is presented at fig. 1. There are two designated positions: position 1 is used for controller, and position 2 is used for timer/commutator module. Full-size 6U RIO-modules are used. An upper (J1) connector is a standard one while the lower (J2) has specialized U/D pins assigned to special functions. The crate is assembled by using a standard upper backplane and a specially developed 7U bottom backplane.

Figure 1: VME-BINP crate front and rear view.

Let us list the additional functions that are added on backplane: intermodule synchronization, intermodule commutation, daisy-chain lines, additional power lines, RIO-Module connectivity.

Synchronization lines include CLK125, USRCLK and SYNC. They are used to transfer a common 125 MHz clock, common user-defined clock and a precise synchronization pulse respectively. LVDS lines routed to each module in such a way that the first 8 positions are aligned better than 100 ps and the total propagation delay to 21st position is less

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than 2 ns. TTL0 - TTL7 – are common trigger/block choose lines that use LVTTL logic level.

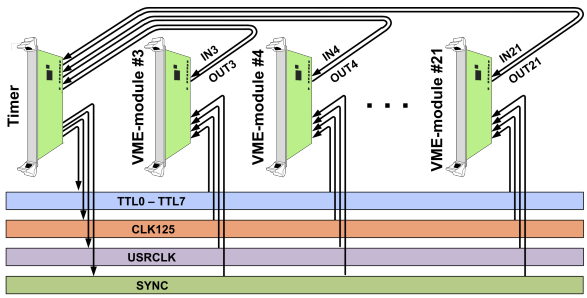

Figure 2: VME-BINP synchronization and intermodule communication.

Intermodule LVDS lines are IN3-IN21 and OUT3-OUT21. They are routed from each module to a timer/commutator position. First 8 positions are aligned better tha 100 ps. Theese lines could be used for fast intermodule communication or synchronization. Timer/commutator is used as a cross-switch for them. The abovementioned lines are presented in fig. 2.

Daisy-chain lines are DI0-DI7, DO0-DO7. They are used to pass signals between consecutive modules and could be used to organize interlock network or some other sub-bus. Each RIO module is a 6U full size (160 mm) board and has 64 connectivity lines RIOA0-RIOA31, RIOC0-RIOC31 from the corresponding front module as well as 12V, -12V, 5V, 3.3 V power lines.

VME64-BINP Crates use a cost-effective ATX power supply. To improve the reliability, each crate is equipped with a status monitor. It provides power state indication, voltage measurement and peak noise detection. Temperature is controlled at two in-crate points. Remote control is possible using CANBUS with reserve power over line.

MODULES

There is a set of VME-BINP compatible modules produced by BINP. Some of them were developed for previous works, and some are new designs.

BIVME2CAN

CANBUS is actively used in BINP automation projects to provide slow control. BIVME2CAN is a module that allows to connect CAN devices to VME Crate. It is a 2-channel module based on SJA1000 chips. Therefore it supports 125 kBit - 1 MBit transfer rates, CAN specification 2.00, has a 1000 packets wide on-board Buffer. A16/D16 addressation is used. CAN4Linux and SocketCAN drivers are available for this device.

VsDC3 Integrator

Ultra-low integration noise level makes this module one of the best in the world. It is widely applied for magnetic measurements with induction coils. The photograph of the module is presented in fig 3, parameters are in the table 2,

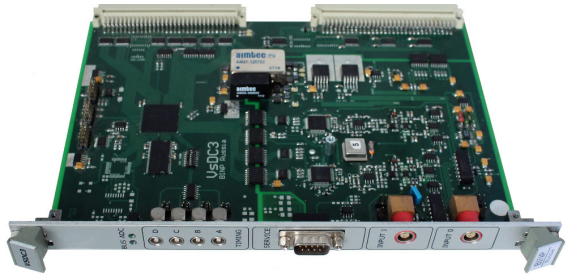

Figure 3: VsDC3 Integrator.

and more detailed description of this module could be found in [4].

Table 2: Main VSDC3 Parameters

Integration Error	10^{-4} ($T_{int} = 5us$)
relative to $U_{range} \cdot T_{int}$	$5 \cdot 10^{-5}$ ($T_{int} = 50us$)
	10^{-5} ($T_{int} = 500us$)
Integration noise	10^{-5} ($T_{int} = 5us$)
relative to $U_{range} \cdot T_{int}$	$5 \cdot 10^{-7}$ ($T_{int} = 500us$)
ADC	24 bits
Nonlinearity $U_{min} \div U_{max}$	$\pm 2 \cdot 10^{-5}$

All devices described hereafter are based on the same template project that was derived from VSDC3 PCB and allowed us to significantly reduce the development effort.

ADC4x250 and ADCx32

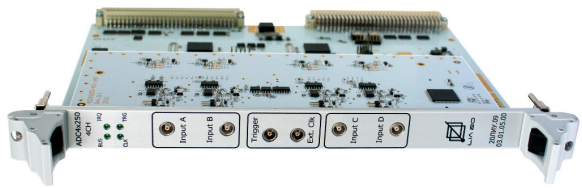

Figure 4: ADC4x250 4 channel version.

These two modules are waveform digitizers. We will provide here only a brief description and an interested reader could find a detailed one in [5]. ADC4x250 is a module with several variants that are based on the same hardware platform. It's picture is presented in fig. 4.

- 1 channel, 1 GSPS, Bandwitdth 300 MHz, ENOB 7.3, 3 MWords memory
- 4 channels, 250 GSPS, Bandwidth 75 MHz, ENOB 10, 786 kWords memory
- 4 channels photodiode, Bandwidth 100 MHz (20 kOhms), SNR 200, amplification 100, 786 kWords memory

ADCx32 is a 32-channel module based on four 8-channel multiplexed ADC's. An ADCx32-RIO is a RIO-module developed to alleviate cable routing. Main parameters of the front module are:

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- four 8-channel ADC's (32 channels)
- up to 125 kSps (switchable)
- 300 kHz bandwidth
- 0.75 MWords/Channel
- ENOB 10.67

S-Timer and L-Timer

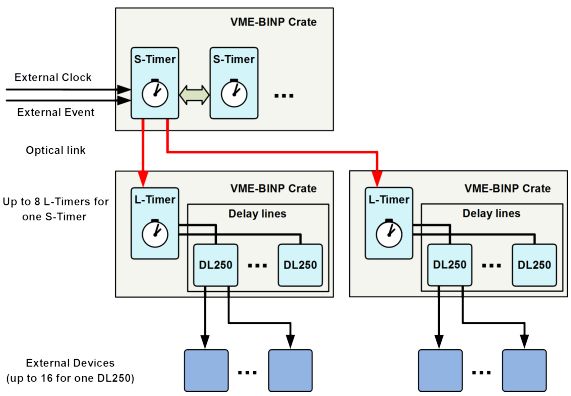

Figure 5: Synchronization structure using Timer modules.

S-Timer and L-Timer allow to synchronize modules in distant VME-BINP crates as shown in fig. 5. S-Timer provides a synchronized 125 MHz clock signal with embedded events data through the optical line to up to 8 L-Timers. S-Timer has an input to receive a precise external clock or external events. Several S-Timers could be united in one crate. The photograph of the module is presented in fig. 6. L-Timer decodes the signal from the optical line and provides all necessary synchronization pulses to the modules of the crate. It also serves as a cross-commutator for LVDS lines. Delay measurement procedure is provided. Both this modules use the same PCB with different montage and are currently in prototype stage.

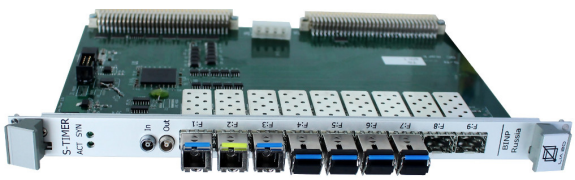

Figure 6: S-Timer.

The main characteristics of S-Timer are:

- 8 output optical lines
- 1 input optical line
- 125 MHz clock in line, 250 MHz internal clock
- ±2 ns Delay measurement error
- 2 synchronization I/O

The main characteristics of L-Timer are:

- 19+19+19 Synchronization lines CLK125, USRCLK, SYNC
- 19x2 LVDS intermodule communication lines
- 8 TTL Lines with 512 ns length
- jitter < 100 ps
- 32 bit counters
- ±2 ns synchronization error

DL-250 and DL-250RIO

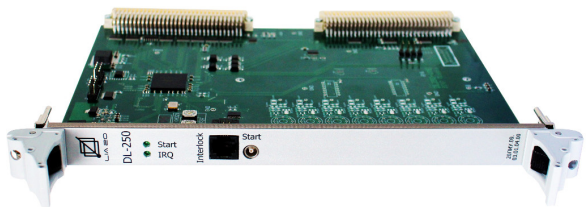

Figure 7: DL250.

DL-250 and DL-250RIO are designed to provide the synchronization pulses for external devices. The photograph of DL250 module is presented in fig. 7. They could work by themselves, or with S-Timer synchronization signals. DL-250 can use Daisy-chain lines as an interlock signal source. Main parameters of DL-250 are:

- External/Program/Backplane start
- Exterental/Backplane interlocks
- 16 channels (RIO) + 8 channels (Front)
- Discrete 4 ns
- Range 17 s
- jitter < 100 ps if synchronous, ±2 ns if asynchronous
- +3.3 V, 10 mA RIO output signal
- 200 mA front output signal
- 0.5 us pulse length
- 5 ns rise time

Main parameters of DL-250RIO are:

- 16 channels
- 200 mA, 10 V at 50 Ohm output signal
- 5 ns rise time
- 30 ns propagation delay
- 500 V galvanic isolation with short-circuit protection

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CONCLUSION

A modification of VME64x standard called VME64-BINP was developed for future automation tasks and upgrade of existing control systems in BINP. A crate and a set of modules were created and produced in small parties(5 - 20 units). We plan to manufacture more than 500 modules of all types and more than 30 VME-BINP crates for the following 2 years to be used in BINP projects. Most of the presented modules are based on the same template project, that allowed us to reduce development effort. A Tango-based software and drivers are provided for all modules [6].

We are also going to develop a VME-controller based on a modern architecture SOM. Currently we are considering TI Sitara ARM for this task. We are considering the development of a “narrow” variant of VME-BINP crate with 8 modules for compact local controllers.

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