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CEA IRFU EPICS ENVIRONMENT FOR THE SARAF-LINAC PROJECT

F. Gougnaud†, J-F. Denis, F. Gohier, T. Joannem, Y. Lussignol
CEA Saclay Irfu DIS, Gif sur Yvette, France

Abstract

Our Institute CEA Saclay Irfu was in charge of providing the hardware and software for the EPICS based control system platform for the accelerator projects Spiral2 [1] at Ganil in Normandy and IFMIF/LIPAc at JAEA/Rokkasho (Japan). Our 3-year collaboration with ESS has given us the opportunity to use new COTS hardware. We have made our CEA Irfu control platform evolve by retaining relevant and evolutive ESS solutions. Currently, CEA Irfu is in charge of the design, construction and commissioning at SNRC(Israel) of the project SARAF-LINAC[2] (MEBT and Super Conducting Linac) including its control. This paper will present our proposition of architecture for the SARAF Linac control system using the new CEA Irfu hardware and software platforms.

INTRODUCTION

Involved in ESS[3][4] controls since 2014, our in-kind and collaborative work with ESS has provided us with new technology knowledge and helped our EPICS platform evolve. We have used the ESS IOxOS VME64X platform for the control of the ESS source at Catania and several ESS test stands at Saclay[5]. This gives us entire satisfaction. Therefore we are giving up the VME/ADAS platform used for Spiral2 and IFMIF/LIPAc for new projects. The IOxOS VME and MTCA solutions offer several seductive assets, the details of which will be provided further on in this paper. The evolution in the PLC domain will also be presented.

CEA is committed to delivering a Medium Energy Beam Transfer line (MEBT) and a Superconducting Linac (SCL) equipped with beam diagnostics (DIA) for supplementing the SARAF Linac accelerator in order to accelerate a 5 mA beam of protons from 1.3 MeV to 35 MeV or deuterons from 2.6 MeV to 40 MeV at the frequency of 176 MHz. CEA is in charge of SARAF-LINAC studies, constructions, tests, installation and commissioning. The new hardware and software platforms are used for the test stands and will be used for the MEBT and SCL controls.

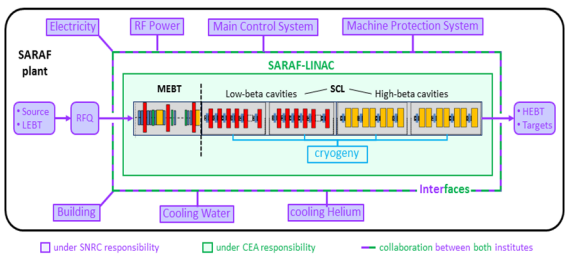

Figure 1: SARAF Linac schematic view.

HARDWARE SOLUTIONS

EPICS Based Hardware

MEBT and SCL controls need fast and semi-fast acquisitions for beam diagnostics and RF signals acquisition. These 2 sets of sampling frequency are needed. The semi-fast sampling frequency is considered from 50KS/s up to 5 MS/s. The fast and semi-fast acquisitions are based on VME64X respectively with the FMC (FPGA Mezzanine Card) boards IOxOS ADC_3110/3111 and ADC_3117.

The CPU IFC_1210, currently used, Freescale PowerPC P2020 based intelligent FPGA controller, will be replaced by the more perennial CPU IFC_1211 that is becoming our standard CPU from late 2017. The IFC_1211 board will be tested on the SARAF test stands in the coming months.

Regarding the IFC_1211 key components, the lifetime is in the order of 15 years.

Long term availability is one of the main advantages of this board IFC_1211 and also the following improvements over the IFC_1210:

- T2081 processor up to 1.8 GHz featuring hardware FPU based on AltiVec for high demanding applications.
- Latest Xilinx FPGA generation (Artix-7 and Kintex UltraScale).
- PCI Express GEN3 direct connection between CPU and UltraScale device.
- FMC VITA57.1 multi-gigabit link up to 12.5 Gb/s with direct support of JESD204B interface.

Furthermore, the small European community of Laboratories using the CPUs of the IOxOS company is growing, which is a sound asset for the future.

Requirements	Sampling/monitoring frequency range	COTS solutions
Fast acquisition	1 MS/s up to 250 MS/s	**VME64X & IOxOS CPU 1210/1211** IOxOS FMC ADC-3110/3111 
Semi-fast acquisition	50 KS/s up to 2 MS/s	IOxOS FMC ADC-3117
Remote I/Os control LAN or serial	100 ms up to 1s	Kontron Industrial PC  EtherCAT Beckhoff(Modbus/Tcp)
Process for vacuum and cryogenics & Remote I/Os & Interlock	100 ms up to 1s	Siemens PLC 1500 & I/O boards/  Fieldbus Profinet & remote I/Os

Figure 2: Choice of solutions.

†francoise.gougnaud@cea.fr

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The preferred I/O interfaces are FMC modules that connect directly to FPGAs. FMC modules take advantage of the intrinsic I/O capability of FPGAs to separate the physical I/O functionality on the module from the FPGA board. This has a number of advantages over traditional designs where the analog and digital parts are put together in a single monolithic design. In our context of perennial projects, using FMC boards permits the evolution of the host module that can be changed while keeping the FMCs and consequently without modifying the cabling.

For remote I/Os, our choice remained the cheap Beckhoff EtherCAT modules with communication based on Modbus/Tcp and consequently simpler for maintenance than the one based on the real-time TwinCAT kernel.

PLC Solution

Programmable Logical Controllers (PLCs) are industrial and reliable devices with a lifetime of at least 10 years, signal versatile and widely used all around the world in industries. For many years our choice has been Siemens because this company is very well known in the research environment, and a lot of hardware and software developed for research, are able to communicate with this kind of PLC. Our Laboratory has developed a very good knowledge of these devices and deployed them on experiments all around the world.

With the growing international context of CEA experiments, we have observed that Siemens is able to offer international support.

Siemens PLCs are divided into several families, from the previous 300 generation, which has worked for more than 10 years, to the new 1500 generation, the possibilities are endless.

In our case, we have chosen the latest 1500 generation, and more precisely the 1516 CPU that gives good flexibility as far as processing power and fieldbus communication are concerned. This CPU is able to communicate with Profinet, Profibus-DP and Ethernet devices.These three interfaces cover a huge quantity of industrial devices that are used on physics experiments. We could take as example vacuum measurement devices like Pfeiffer TPG300 or Brooks SLA5850S for helium flow regulation which communicate with the Profibus-DP standard.

This 1516 CPU has many fieldbus-link possibilities, but also has to be connected to sensors and actuators, which are not fieldbus compliant.

For these devices, analog and digital I/O cards are available to interface with industrial standard signals. They are able to read 0-10V, 4-20mA, 24V signals and a lot of other kind of signals. For outputs, possibilities are pretty similar. These few cards give a high flexibility to the system and also provide easy maintenance because of only four references to provide, one by kind of signal (analog input or output, digital input or output). With a 14-bit reading range signal, high precision control and regulations are easy to implement.

As previously mentioned, PLCs are robust devices not only for hardware but also for software. Languages used are worldwide industry standards like Ladder or Grafcet, for automatic procedures and SCL or List for extended functions. These devices don't have a dynamic memory allocation. Each bit has its own position, defined by the programmer and will never move in the memory architecture. This technology provides PLCs with a long life expectancy.

IRFU EPICS ENVIRONMENT (IEE)

The Irfu EPICS Environment aims at configuring, in an identical way, all the computer systems for development and operation, by installing the same distributions of Linux packages and the same version of EPICS software. Furthermore, it provides a standard EPICS development environment and software module templates that must be used as containers for new developments. A development and a production workflow is also strongly recommended.

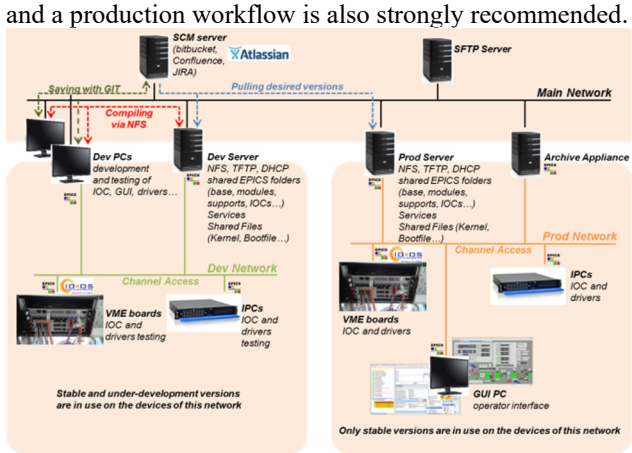

Figure 3: Development workflow.

System Architecture

IEE is based on a client/server architecture. Clients can be PCs, industrial PCs (IPC), or VMEs.

Servers can be run inside a Virtual Machine. This design will also be extended to the Development PCs. Servers and development PCs are connected to a main network. Servers are also connected to a private subnetwork for VMEs and IPCs boot and Channel Access communication.

The "CentOS" distribution is installed on each main server and development PC. In order to have a common development environment an Ansible Playbook is provided and does the installation from Linux. For a main server the playbook configures each service and each file to be shared automatically. For a development PC the playbook allows to get all the shared files and tools from the main server.

The architecture of an IPC is based on the X86 standard, like a PC. It is more robust and without a fan. In this case, it doesn't need a graphical user interface. So the installation uses the same "CentOS" distribution as a PC but without graphical libraries.

In order to have the same distribution, all IPCs boot on the network. From the main server, all necessary files (Kernel, Uboot file) are downloaded by TFTP and the common rootfs is mounted by NFS.

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The Linux VME platform requires a cross-compilation chain for the PowerPC architecture. The Embedded Linux Development Kit (ELDK) and the Yocto project, based on OpenEmbedded, are used. Yocto was chosen because of its versatility.

In the same way as IPCs, the VMEs boot on the network. From the main server, it downloads all needed files (Kernel, Uboot file) by TFTP, and it mounts the common rootfs by NFS.

EPICS software platform

The EPICS Software Distribution is a selection of Base, IOC support modules and extensions found on official EPICS sites. The currently used EPICS Base is R3.15.4. The IOC support modules are categorized as either Soft Support or Hardware Support. The extensions are host tools and Channel Access clients such as Control System Studio (CSS), Archive Appliance, CA libraries (Java, Python…). This distribution software is installed on the Control System NFS Server and diffused on all development PCs.

The development environment fully relies on the standard EPICS Build Facility. EPICS software can be divided into multiple <top> areas. An example of a <top> area is the EPICS Base itself. Each <top> may be maintained separately. A <top> directory structure essentially contains the build configuration files in a configure folder and a Makefile. Other subdirectories depend on the destination of the <top> area.

The GUIs rely on CSS BOY.

EPICS Development Model

The Irfu EPICS Environment provides a standard development model that should be adopted by all the developers involved in the control system software for SARAF. These standards give the necessary homogeneity to the software modules produced.

The following makeBaseApp template structures cover the needs for IOC development:

- A Top Directory dedicated to developments.
- A Support Application template.
- An IOC Application template.

The Support Application template creates under the <top> directory a module structure <my-app>App to organize software sources, database definitions, template databases, graphical user interfaces, and so on, related to an accelerator function or device. It contains makefiles suitable to build Linux libraries and applications and to install files into <top> subdirectories. It has the following directory structure:

```
<my-app>App
├── ChangeLog
├── Makefile
├── README
├── db
│   ├── Makefile
│   └── {*.db, *.template, *.substitutions, *.proto}
├── doc
│   └── *.pdf
├── misc
│   └── {*.xml, ...}
├── opi
│   ├── *.opi
│   ├── pictures
│   │   └── {*.jpeg, *.png, *.tiff, ...}
│   └── scripts
│       └── {*.js, ...}
├── src
│   ├── Makefile
│   ├── <my-app>App_Include.dbd
│   ├── <my-app>App_Support.dbd
│   ├── doxygen.cfg
│   └── {*.c, *.h, *.st, ...}
└── test
    └── {*.py, ...}
```

The IOC Application template creates a module structure ioc<My-ioc> under the directory <top>/iocBoot to organize operational databases, startup scripts, and so on, for an IOC application. It contains makefiles suitable to define which support libraries are used by the IOC application and to build it. It has the following directory structure:

```
ioc<My-ioc>
├── ChangeLog
├── Makefile
├── README
├── boot
│   ├── Makefile
│   ├── ioc<My-ioc>.cmd
│   └── ioc<My-ioc>_connections.cmd
├── db
│   ├── Makefile
│   ├── ioc<My-ioc>.req
│   └── ioc<My-ioc>.substitutions
├── misc
│   └── {*.xml, ...}
└── src
    ├── Makefile
    ├── ioc<My-ioc>Include.dbd
    └── ioc<My-ioc>Main.cpp
```

SARAF LINAC ARCHITECTURE FIRST STEPS

To manage and synchronize the studies with the different phases of the project, we have divided the CEA scope control system of the SARAF Linac into 4 parts: MEBT, Super Conducting Linac (SCL), LLRF and Diagnostics control systems. SNRC is responsible for the Machine Protection System and the Timing System. Several test stands are being built with their control system to test the design and the chosen technologies in the different technical domains. For instance, the first test stand is dedicated to the RF conditioning of cavities' couplers. The control uses the IEE with IOxOS boards for the semi-fast RF

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acquisition and Beckhoff modules to read some thresholds and temperature sensors. The tests will start next November.

MEBT ARCHITECTURE OVERVIEW

The control of the MEBT itself is relatively simple. It has to control power supplies for quadrupoles and steering magnets, vacuum and the 3 brushless motors of the 3 rebunchers. The EPICS IOC is dedicated to the communication with PLCs and to the slow control of the power supplies and temperature sensors. When the diagnostic control including fast acquisition is integrated, a VME will be added and may replace and take in charge the IPC control. There are 2 PLCs, one is dedicated to vacuum control and the other to rebuncher tuners. The interlock chain has not been defined yet. Early 2018, test stands dedicated to the rebuncher prototype and the power supplies will be installed, which will enable us to partially test the MEBT control. In 2019, the MEBT control system should be completely tested at CEA Saclay.

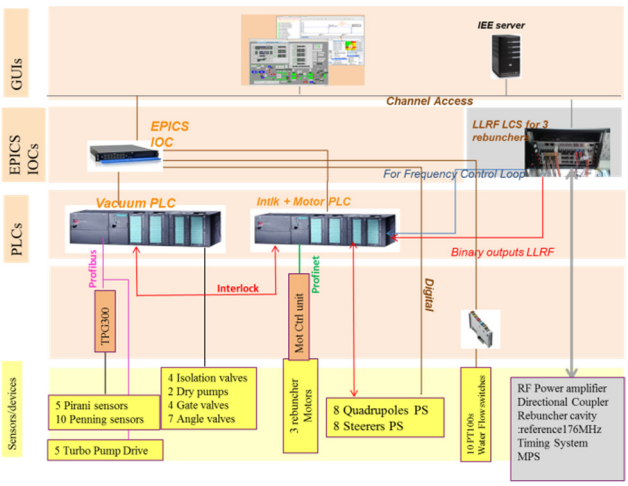

Figure 4: MEBT architecture overview.

SCL CRYOMODULE ARCHITECTURE

The SCL will include 4 cryomodules, including 2 cryomodules with 6 low-beta cavities and 2 other cryomodules with 7 high-beta cavities. Several test stands will be built to test SARAF cryomodules and cavities with their control from 2018 to 2020.

SARAF Cryomodule Test Stand

The ESS elliptical cavity cryomodule prototype test demonstrator (ECCTD) has been designed, built and tested at CEA. This prototype is controlled by a system composed of PLC and EPICS devices. EPICS manage the fast acquisition part like RF and Piezo systems, called "fast" signals. PLCs are connected to cryogenic, vacuum, stepper motor sensors and actuators, called "slow" signals. Slow and fast technologies work together in the same cryomodule control system and were validated for the ESS ECCTD in late August 2017. The SARAF cryomodule test stand will be located near the ESS one and will benefit from this proximity.

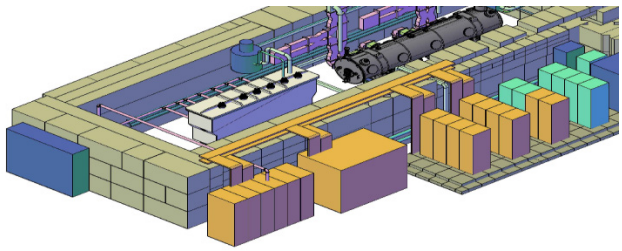

Figure 5: CEA experiment area with ESS (green) and SARAF (orange) cabinets.

In fact, cryogenic interface system, based on PLC, was made in order to enable the communication and cryogenic liquid flow between cryoplant and cryomodules for control validations. This cryogenic interface, deployed for the ESS cryomodule qualifications phases, gave us the possibility to simulate a valve box and to make the cryomodule control work in a similar way to the one that will be deployed at the ESS accelerator.

The context for the SARAF cryomodules is similar and the same philosophy of cryogenic interface will be followed.

Saraf Cryogenics PLC Use Case

Generally speaking for a cryomodule, PLCs control cryogeny, vacuum and interlocks. In this paper only the cryogenic control will be addressed. Using cryogenic liquids, like helium or nitrogen, requires specific devices, for instance for temperature measurements.

For common temperatures, PT100 sensors are reliable and very precise, down to 70°K. Below this point, another technology is used: Cernox sensors. PT100 sensors can be connected to PLC analog cards, but not Cernox sensors. In order to read them, a signal conditioner is used, the CABTR device from Seico company. It can read eight Cernox channels and communicate the values to a PLC via Profinet. Thanks to this standard industrial fieldbus, native for PLC CPU, communication is secure, quick and precise. As PT100 sensors have a wide measurement range, they are used as much as possible for ambient temperatures and also top level cryogenic systems, where nitrogen is used or when helium is not in liquid form. They are used on the thermal shield for example, where temperatures are not too low for them. For cavity temperature measurement, Cernox sensors will be used because of the liquid Helium cryogenic environment.

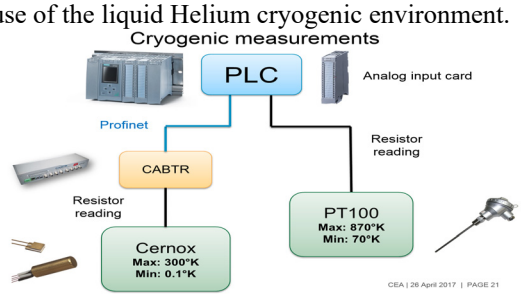

Figure 6: Cryogenic temperature measurement architecture with a PLC.

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Architecture at Soreq for Cryogenic Control

PLCs have to control cryomodule cryogeny, vacuum and local cryoplant communication. The CEA test stands will be composed of a cryomodule, but not of the Soreq SARAF cryoplant. In order to reduce the possibility of software errors and improve reliability, the control system developed at CEA Saclay has to be as similar as possible to the SARAF configuration site at Soreq. To follow this philosophy, one PLC will be dedicated to each cryomodule, like on the test bench. Another PLC will ensure communication with the local cryoplant at the Soreq site.

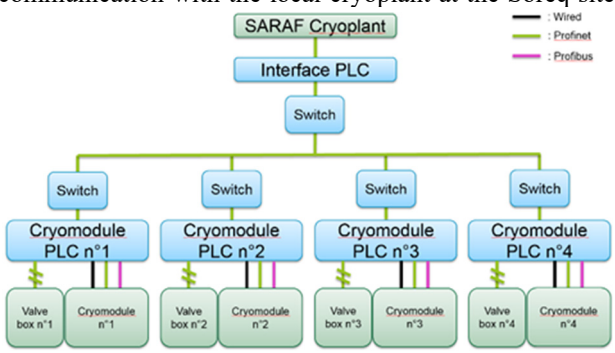

Figure 7: Main PLC architecture for SARAF cryomodule.

The Cryomodule PLCs have their own architecture. In fact, more than 60 temperature sensors, 12 vacuum gauges, 18 analog valves and a host of other sensors and actuators have to be controlled for each cryomodule. Some elements are far away from the main part of the control system. In order to enable control, remote I/O systems, called ET200MP will be used.

Using Profinet, these devices provide an extended network, via Ethernet cables. For example, valve boxes will be far away from the main cryomodule control system. An ET200MP will be connected to the Cryomodule CPU via Profinet and will be composed of cards dedicated to temperature measurement and valve control.

As you can see on figure 8, Profinet connects most of the devices, the others are Profibus devices.

The vacuum interface called TPG300 from the Pfeiffer Company also communicates with this standard.

Signal conditioning systems such as CABTR are located near PLC CPU, in cabinets. This choice is justified by EMP (Electro Magnetic Pulse) protection, to simplify internal cabling and network.

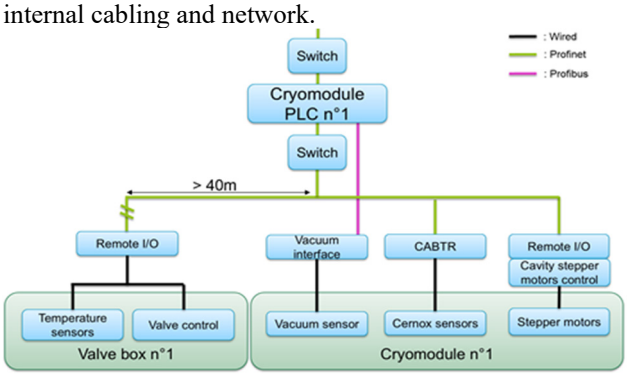

Figure 8: Cryomodule PLC architecture with sensors and actuators.

CONCLUSION

We have been polishing the stability of the EPICS environment platform for the SARAF control system for several months. This environment is simple and does not need significant human resources for maintenance. The Irfu control system team gathers EPICS and PLC experts who are used to working together and providing integrated controls for fast and slow signals. All GUIs are based on CSS BOY which produce a homogeneous operator interface.

A close collaboration with Soreq colleagues and many exchanges is needed because of the numerous interfaces. First exchanges are fruitful and collaboration for this new machine is attractive. The SARAF Linac control system is a very challenging project. The installation of the MEBT controls including diagnostics is planned for early 2020 and the installation of the SCL and diagnostics for 2021. The different test stands enable all the subsets of the MEBT and SCL control system to be tested.

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