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OPTIMISATION OF A LOW-NOISE 1.3 GHz PLL FREQUENCY SYNTHESISER FOR THE EUROPEAN XFEL

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Abstract

The Master Oscillator system of the European XFEL was built using frequency synthesis techniques that were found to have the best phase noise performance. This includes low noise frequency multipliers and non-multiplying phase lock loops, incorporated in the system to shape its output phase noise spectrum. Jitter of the output signal strongly depends on phase noise transmittance of the PLL and suboptimal design can worsen it by orders of magnitude. Taking into consideration that the PLL open loop transmittance usually can be shaped in multiple ways, and that the accurate phase noise measurements can easily take more than 30 minutes, designing an automated tool becomes a necessity. For this purpose an approach to the tuning system construction was chosen in order to make the phase noise optimisation process simpler. This paper describes the optimisation of PLL synthesizer phase noise, done to improve the performance of the European XFEL MO. We present the phase noise optimisation process and achieved results.

INTRODUCTION

Master Oscillator [1] is a low noise and high power reference signal generator for the European XFEL [2] (X-Ray Free Electron Laser) which was built in the DESY Institute in Hamburg [3]. System consists of three structurally identical generation channels, and a redundancy module designed to detect the failure of a generation channel and optionally change the output signal source. In this application, a very low phase noise of the 1.3 GHz reference signal is required to assure high precision of the accelerating field control. Therefore single MO channel incorporates a frequency synthesizers chain, starting with a GPS Disciplined Rubidium Oscillator (10 MHz), followed by a phase locked oscillators: 100 MHz OCXO (Oven Controlled XTAL Oscillator) and a 1.3 GHz DRO (Dielectric Resonator Oscillator). Apart from using high performance VCOs (Voltage Controlled Oscillator), big effort was also put on choosing the frequency conversion methods and a PLL (Phase Lock Loop) synthesisers parameters.

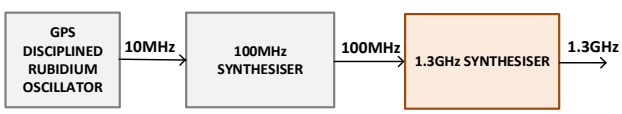

Figure 1: XFEL Master Oscillator block diagram. The optimised synthesiser is highlighted.

The following article describes the process of 1.3GHz PLL synthesiser tuning performed to improve the Master Oscillator output signal phase noise performance.

PHASE NOISE AND A PHASE LOCK LOOP

Phase noise is often one of the most important parameters of a frequency generator [4]. Output signal of an RF signal generator may be described as a pure sine wave modulated by both amplitude and phase noise. In case of RF oscillators, the phase noise usually dominates over the amplitude noise, so all of the further presented considerations will concern only the phase noise, which actually represents the signal short-term phase/frequency stability. The most common way of presenting the oscillator's phase noise is a ratio of the spectral power density measured in 1 Hz band at a specified offset frequency from the carrier to the total power of the carrier signal [5]. An example of a real oscillator phase noise characteristic is presented on Fig. 6 (yellow plot, "free-running VCO"). Stability of the generated signal may be also described using a jitter parameter – phase noise integrated in specific bandwidth.

Phase Lock Loops [6] (Fig. 2) are used to synchronize the VCO frequency and phase to the reference signal. PLL consists of three main functional blocks: phase detector, loop filter and the VCO. Phase detector output voltage is proportional to the phase difference between reference and VCO signal. In perfect case (without the noise) the signals are synchronized and the filtered phase detector output signal (VCO control signal, U_{VCO}) is a DC voltage. In real system, where both signals are modulated by the phase noise and each loop component adds its own residual noise, it contains also an AC component – an incidental, noise-caused phase difference between both signal phases, multiplied by the phase detector sensitivity and the loop filter transmittance. VCO control signal is tuning the oscillator in order to minimise the phase difference detected by the phase detector, closing the negative feedback loop.

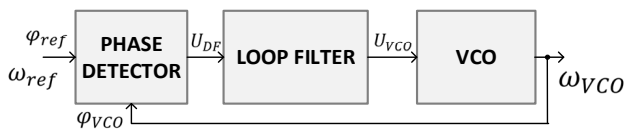

Figure 2: PLL block diagram.

The phase noise characteristic of the PLL output signal can be shaped by adjusting the loop filter (low-pass filter) transmittance. For low offset from carrier frequencies, where the phase detector signal is not attenuated by the PLL transfer function, the VCO phase is tracking the reference signal phase – which means, that even if the free-running oscillator output phase noise is high, inside the

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loop bandwidth, the PLL output signal phase noise is similar to the level of reference signal phase noise. Similarly, for high offset frequencies, the PLL output phase noise equals the free running VCO phase noise, and between, close to the PLL cut-off frequency, it is a combination of both phase noise sources.

OPTIMISATION TECHNIQUES COMPARISON

Two different ideas for design of a phase noise optimiser were considered. First one was based on equations describing the PLL open and closed loop transmittances. It allowed to calculate the PLL's output phase noise using the measurements of loop components parameters. Required parameters are at least the phase detector sensitivity, loop filter transmittance, VCO tuning sensitivity or the free running VCO and reference signal phase noise. In second method an opposite approach was applied: replacing the loop filter components with digitally controlled variable resistors or capacitors. The main pros and cons of both approaches are collected in the Table 1. Finally, physical system optimisation approach was chosen as more convenient in our application.

SYSTEM DESIGN

The simplified block diagram of the 1.3 GHz synthesiser with attached optimising system is presented in Fig. 3. The optimised 1.3 GHz phase lock loop, installed as a last frequency synthesiser in the chain, is used to lower the synthesisers output phase noise by combining the close-to-carrier noise of the multiplied 100 MHz signal with low far-from-carrier noise of the 1.3 GHz VCO. In this case loop filter was implemented as an active integrator in order to keep the DC phase error at zero. The filter transmittance has two time constants - one pole and one zero, which defines the loop bandwidth and damping factor. Generally, in order to manipulate the two time constants it is enough to vary two of three values of components. However, because of the op-amp voltage and current noise (their impact on the filter output noise depends on the resistor values) and phase detector gain dependency on resistive and capacitive load, three digitally controlled variable resistance/capacitance tuners were installed.

Table 1: Pros and Cons of Different Approaches to the Optimisation

Theoretical model optimisation	Physical system optimisation
+very fast – usually below 10min -each model is custom, cannot be re-used -model construction is difficult and long process, -model needs actualisation after every component exchange	+once designed optimising tool can be universally used -very slow – optimisation can easily last few hours -signal source analyser is occupied all the time -connection of additional system into the signal path – possible parasitic capacitance/inductance and EMI problems -isolated environment required – single distorted measurement can misdirect the optimising tool

The optimising system, consists of three main parts: the system controller, tuners and a phase noise analyser. Presented system structure was developed to possibly minimise the error caused by impact of connecting external equipment to the system. For that reason variable resistance/capacitance tuners (Figures 4 and 5) consist of discrete resistors/capacitors, switched with deeply saturated MOS transistors. It was impossible to totally avoid parasitics, therefore non-negligible values were characterized. The last big concern was the EMI – signals induced in the wires, observable in the phase noise as a discrete (spurius) lines. They are easily identifiable, because pure output signal values for neighbouring offset frequencies are similar. Therefore in the performed optimisation, spurius lines were removed.

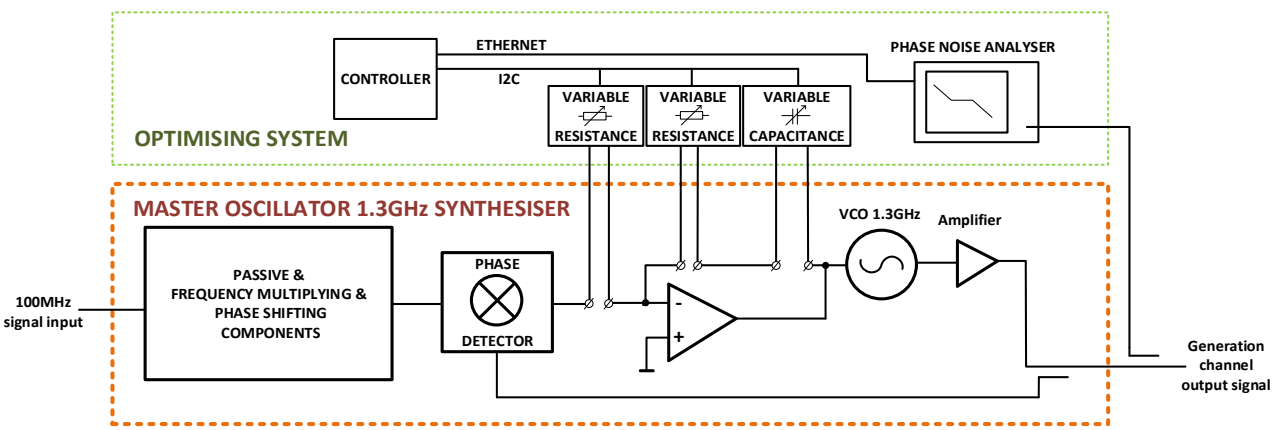

Figure 3: Block diagram of the optimising system.

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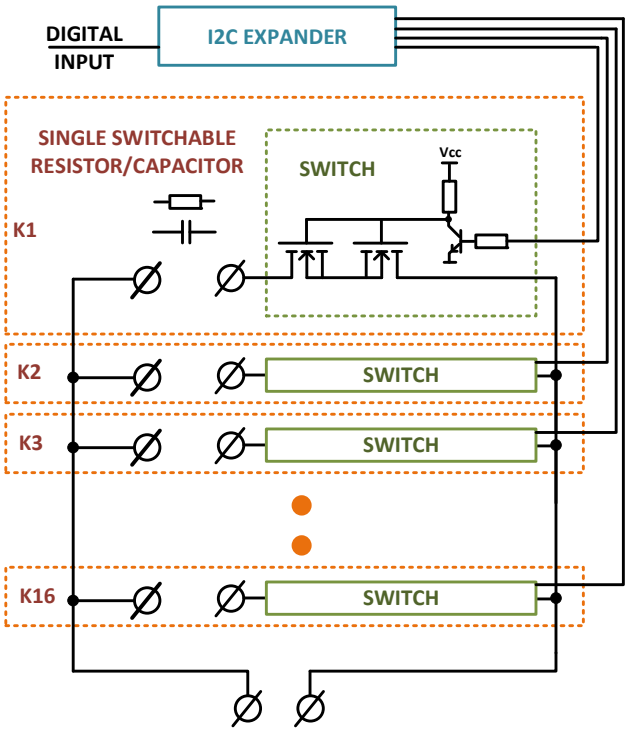

Figure 4: Single variable resistance / capacitance tuner block diagram.

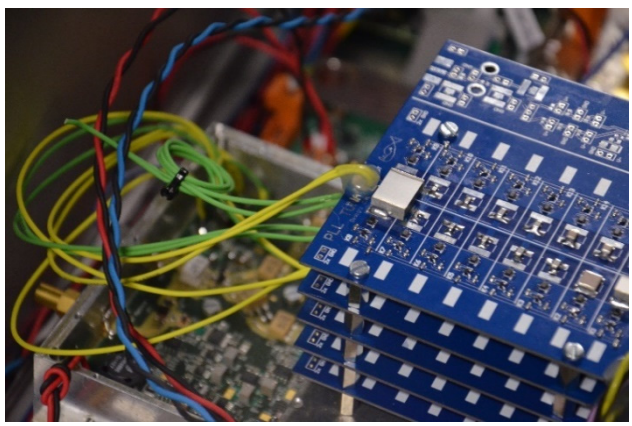

Figure 5: Tuners connected to the Master Oscillator 1.3 GHz Synthesiser PLL.

For optimisation purposes, interface of the control and measurement system was represented as a goal function with loop filter parameters (R and C values) as arguments. It was decided to set the PLL output signal's random jitter as a function's output value, because it's a single real number that well describes the signal short-term phase stability. One of the most important goal function parameters was the integration bandwidth of the random jitter, which could lead to suboptimal optimisation result, if selected inappropriately. Because of measurement uncertainty of the phase noise analyser, very wide integration bandwidth (because of higher close-to-carrier phase noise this applies especially to integration start frequency) means also increased random jitter measurement uncertainty – the observed change of signal random jitter caused by the loop filter transmittance modification (wanted change) is more affected by the measurement error, than when the integration bandwidth is narrow. On the other hand the integration bandwidth had to be wide enough to avoid the situation when modification of the filter component values results in increased random jitter outside the integration bandwidth. Finally, by way of an experiment, it was set to range of 300 Hz — 1 MHz, and resulted in the measurement accuracy of around 0.05 fs (defined as 6σ estimated of 30 measurements). No random jitter increase outside of the integration bandwidth was observed. For the optimisation, the Nelder-Mead algorithm, implemented in the Matlab function fminsearch() [7] was used. The algorithm uses a derivative-free method and is recommended for solving problems where goal function output value is affected by a measurement uncertainty. Its main disadvantage is only local region of search, therefore good selection of optimiser start point was necessary. Two optimisation stop conditions were set. The first, termination tolerance on the function value, was satisfied when random jitter improvement in an iteration was smaller than 0.35 fs, and was necessary due to finite accuracy of the measurement device. The second, termination tolerance on optimised vector, when a change of optimised values in an iteration was smaller than 20 Ω or 20 nF, was used to avoid situation when step of the optimiser is smaller than resolution of the variable resistance and capacitance tuners. The start value was chosen experimentally.

OPTIMISATION RESULTS

The phase noise plots before and after the optimisation are compared on Fig. 5. Optimiser improved the PLL output signal random jitter measured in 300 Hz … 1 MHz bandwidth from 2.21 fs to 1.98 fs, and has proofed its usefulness in loop-filter optimisation of ultra-low phase noise PLLs. Comparing to the free-running VCO, PLL output signal phase noise contains few more spurious components. Taking under consideration that the spurious lines do not change their positions when the loop transmittance is modified, they are expected to have their origin in EMI problems introduced by connecting the external tuners to sensitive nodes in the PLL. Although, they do not distort the optimisation (the phase noise analyser is able to measure the random and discrete jitter separately, and the value that the optimiser read out of the analyser is just the random jitter). Because of very satisfying optimisation results, tests of dependencies between the start vector values and the optimisation result (searches for a better local minimum) were not performed.

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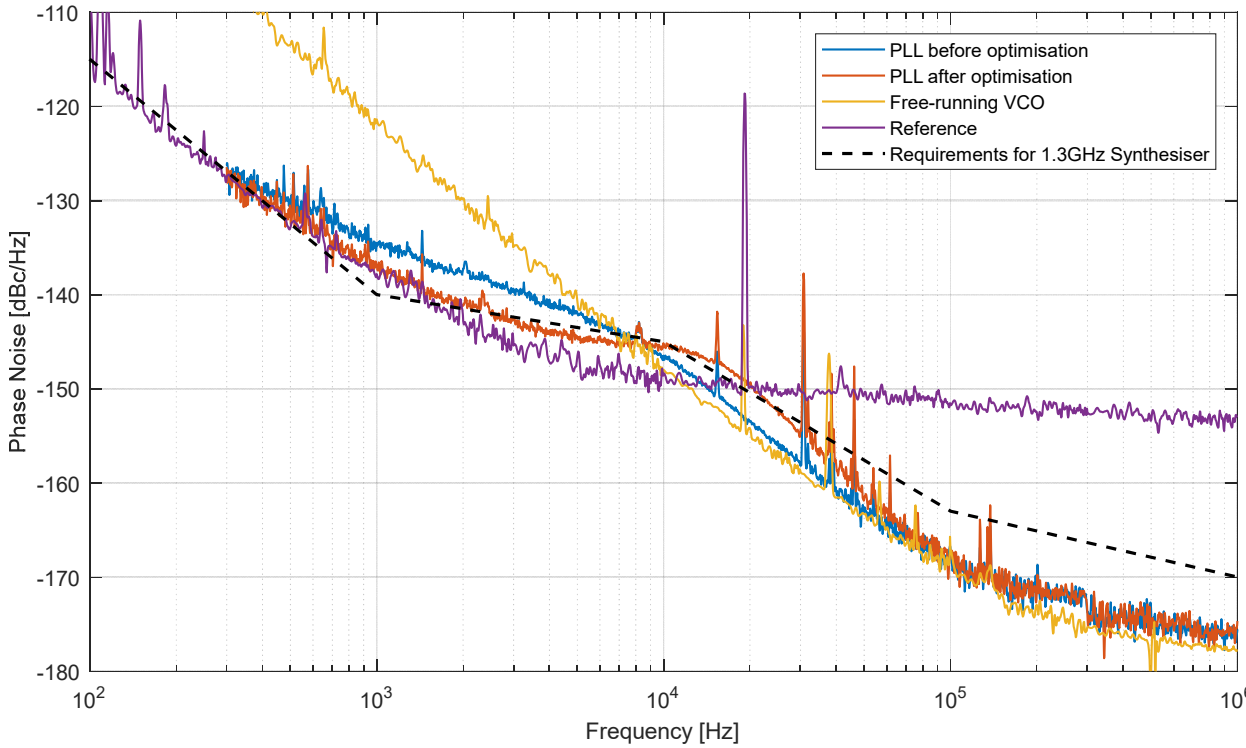

Figure 6: Compared phase noise measurements: reference signal, free-running VCO and PLL output signal for the optimised vector start and end values.

CONCLUSIONS AND PLANS

During the optimiser design, two different ideas for construction of the system were considered and one of them, physical system optimisation, was chosen. The optimising system construction process contained design of the digitally controlled variable resistor/capacitor tuners, selection of goal function and preparation of the software. The tests prove the system usefulness in optimisation of high performance PLL phase noise. In the future experiments with different goal functions and optimising algorithms will be conducted in order to shorten the optimisation time and make the tool more accurate and universal.

ACKNOWLEDGEMENT

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REFERENCES

[1] L. Zembala *et al.*, "Master Oscillator for the European XFEL", in *Proc. 5th Int. Particle Accelerator Conf. (IPAC'14)*, Dresden, Germany, June 2014, paper WEPRI116, pp. 2771-2773.
[2] E-XFEL, https://www.xfel.eu/.
[3] DESY, https://www.desy.de/.
[4] E. Rubiola, "The Leeson Effect", *European Frequency and Time Forum*, Neuchatel, Switzerland, May 2014.
[5] K. Gheen, "Phase Noise Measurement Methods and Techniques", webcast, Agilent Technologies, 2012.
[6] Dan Wolaver, *Phase-Locked Loop Circuit Design*, Prentice Hall, 1991.
[7] MATLAB and Optimisation Toolbox Release 2017b, The MathWorks, Inc., Natick, Massachusetts, USA.