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MicroTCA GENERIC DATA ACQUISITION SYSTEMS AT ESS

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Abstract

The European Spallation Source (ESS) is a Partnership of 17 European Nations committed to the goal of collectively building and operating the world's leading facility for research by use of neutrons by the second quarter of the 21st Century. The strive for innovation and the challenges that need to be overcome in order to achieve the requested performances pushed towards the adoption of one of the newest standards available on the market. ESS has decided to use MicroTCA as the standard platform for systems that require high data throughput and high uptime. The implications of this choice on the architecture of the systems will be described with emphasis on the data acquisition electronics.

INTRODUCTION

For many years VME has been the preferred choice in the accelerator and science community for data acquisition systems. The availability of many manufacturers, who developed either crates or boards, the reliability of the platform, proven in both industrial and research environments, and the established knowledge base of the system acquired during the years by many engineers made the selection of this standard a safe choice.

In the last decade quite a few new standards started to challenge VME for both scientific and industrial applications, a few examples could be the ATCA for telecommunications, OpenVPX for military and aerospace, PXI and MicroTCA for measurement and automation applications. All of these new standards share the characteristic of replacing the old parallel architecture of the buses with newer ones based on serial interconnects, like PCIe and SRIO, leveraging the technological advances and the increasing availability of multi-gigabit transceivers in many silicon devices including FPGAs.

MicroTCA Capabilities

MicroTCA is defined as a complimentary standard to ATCA (Advanced Telecommunications Computing Architecture) and its purpose is to address cost sensitive and physically smaller applications while still retaining most of the underlying philosophy, interconnect topologies and management features [1, 2].

MicroTCA infrastructure is designed to provide high availability, the standard itself claims that its goal is to achieve an up-time requirement of 99.9%. This characteristic is achieved through the integration of features for resiliency, redundancy, serviceability and manageability. MicroTCA uses IPMI with the addition of PICMG specific commands to manage the system components. The MicroTCA Carrier Hub (MCH) features a MicroTCA Carrier Management Controller (MCMC) whose role is to monitor and control the Advanced Mezzanine Cards (AMCs) that are part of a shelf by means of the IPMB-L bus as well as presence detect and enable signals. By interacting with the MCH it is possible to disable and start any specific Field Replaceable Unit (FRU) in the crate and to monitor the sensors provided on each card. According to the standard the management section shall be able to supervise the available supply voltage levels and the temperatures of critical areas on the PCB like those close to the air inlet and outlet and core components. In addition to these sensors it is also possible to monitor the connectivity status of each card, both on the Fat Pipe Region and on the GbE interface. Thresholds can be set for each of the cards to allow the MCMC to take actions and warn the user if a monitored parameter is drifting away from its nominal value.

The use of AMCs, the same equipment that can be used with certain restrictions in the ATCA environment by means of ATCA carrier cards, as the basic building blocks of the MicroTCA system allows migration between the two platforms. The manageability, modularity and hot-swap capabilities provided by the infrastructure allow the standard to be flexible, by configuring diverse AMCs in a MicroTCA shelf many different application architectures can be realized. The availability of infrastructure components that provide switching capabilities for different protocols like PCIe, Ethernet and Serial Rapid IO further expand the range of applications that can be covered by this standard [3].

MicroTCA makes provision for up to 4 telecommunication clocks on the backplane, plus one additional fabric clock to be used as the reference for the aforementioned interconnection standards, and up to 20 full-duplex ports (differential TX and RX links) that can be used to move data amongst the different AMCs or towards external systems. Common backplane implementations provide redundant Gigabit Ethernet (GbE) communication links on AMC ports 0 and 1 and direct board to board connections on ports 2 and 3 (ie. SAS/SATA). The main communication channel, called Fat Pipe, uses ports 4 to 7 whereas the Extended Fat Pipe, which is used when redundancy or higher bandwidth is required, is implemented on ports 8 to 11. Ports 12 to 20, exception made for port 16, are the so called Extended Options Region and are further divided into two sets. Ports 12 to 15 are usually reserved for additional direct AMC to AMC connections whereas a M-LVDS bus implementation uses ports 17 to 20. Port 16 is used for two out of the four total telecommunication clocks.

Figure 1 shows an overview of an implementation of a MicroTCA backplane used at ESS.

ESS has adopted a multi-layer strategy for implementing the data acquisition and control systems with different architectures covering complimentary input signal frequencies and response time. For the majority of applications with

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input signal frequencies above few tens of kHz a MicroTCA based system will be used.

OVERVIEW

The ESS project depends on the results of many in-kind contributions provided by a large number of institutes of the European country members. The in-kind nature of the project is reflected in the list of hardware modules that are going to be used to implement the different instruments, equipment that will complement the Customer Off The Shelf (COTS) components already available.

The relevant system owners at ESS have indeed decided, after careful evaluation, to rely on currently available COTS MicroTCA infrastructure components like chassis, power modules, MCHs and CPU cards. The tested equipment fulfilled the requirements of the many instruments relying on this architecture. PCIe has been selected as the interconnection standard to be used in the Fat Pipe Regions.

At the time of this paper the number of MicroTCA systems to be deployed in the facility is estimated to be less than 500 [4], these many systems will be grouped and located into rack islands along the roughly 600 m, from ION source to Target Station, of the ESS linear accelerator. The list of systems (devices) that will rely on the MicroTCA infrastructure can be divided into four categories: Beam Diagnostics, RF Systems, Machine Protection and Timing System.

Beam Diagnostics category includes systems like the Beam Current and Position Monitors, Beam Loss Monitors, Emittance Meters and Wire Scanners. RF Systems comprise Low Level RF and RF Local Protection Systems (RF-LPS). Machine Protection will implement a subset of the Fast Beam Interlock System decision logic using AMC cards. Timing System services are required by all previous categories and Event Receiver AMC cards will be deployed accordingly [5].

Platform Components

The foreseen list of hardware components required to implement the many systems can be divided into two sets, Basic Infrastructure, whose components will be the basic building blocks of all systems, and Application Specific Hardware like AMCs, FMCs and RTMs.

Basic Infrastructure

- *9U Chassis*: Schroff COTS 9U crate hosting up to 12 AMC cards and RTMs, 4 power modules and 2 MCHs. Backplane with dual star topology, direct connections for S-ATA/SAS, clock and trigger lines as per PICMG MicroTCA.4.
- *3U Chassis*: Schroff custom 3U crate hosting up to 6 AMC cards and 4 RTMs, redundant power modules and 1 MCH slot. In order to optimize rack allocation in the accelerator gallery and to accommodate those applications where the use of a 9U crate would be cost inefficient, ESS has requested to the crate manufacturer companies to provide a small 3U crate with a front to rear cooling scheme, product not yet available on the market. The developed chassis provides a backplane (see Fig. 1) that closely mimics the first half of the 9U crates interconnections but provides doubled bandwidth for PCIe by means of a single MCH. The increase in available throughput is achieved by merging the Fat Pipe and Extended Fat Pipe Regions together and by routing ports 8 to 11 of the 6 supported AMCs to the otherwise unused fabrics, due to the reduced number of AMC slots, of the Carrier Hub. The 2 available Power Module (PM) slots allow for power supply redundancy [6].

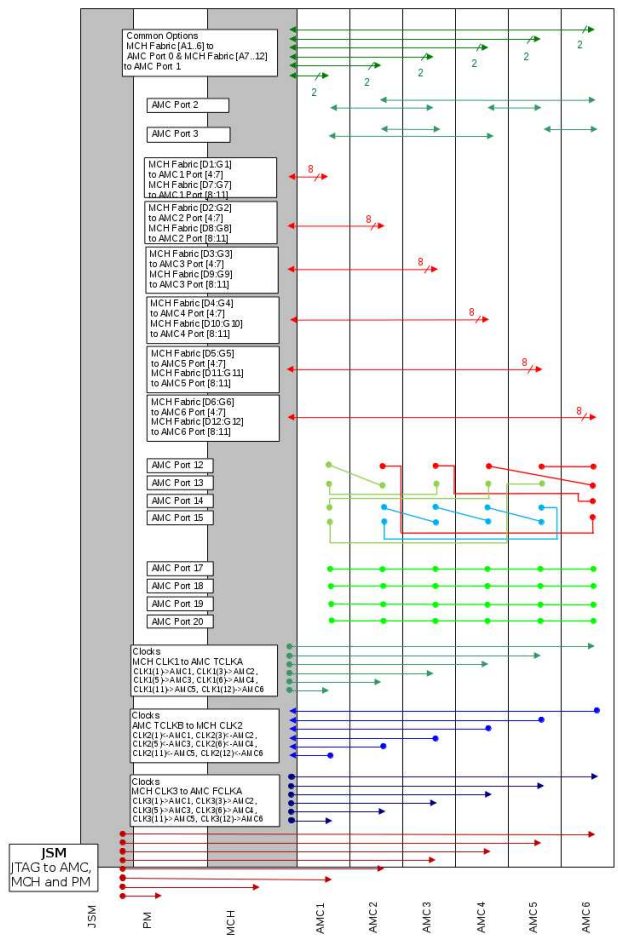

Figure 1: 3U crate custom backplane.

- *NAT-MCH-PHYS*: NAT COTS Carrier Hub that provides a 48 ports PCIe switch, GbE switching for Fabric A (ports 0 and/or 1 of the AMCs) and 2 Ethernet RJ45 interfaces on the front panel. The MCH can drive/receive clock signals on ports CLK1 and CLK2 and supplies the fabric reference clock for the PCIe interface.
- *NAT-PM-AC600D*: NAT COTS 600W PM.
- *MTCA 4.0 1000W PS*: WIENER COTS 1 kW low noise and ripple PM.
- *AM 900 CPU Card*: Concurrent Technologies COTS AMC processor module based on Intel processors.

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Application Specific Hardware

- *MTCA-EVR-300U*: Micro Research Finland AMC Event Receiver card. The board is capable of driving/receiving Telecommunication clock lines TCLKA/TCLKB and to send and get trigger signals on backplane M-LVDS lines. This card will be deployed in many different systems.
- *IFC1410*: IOxOS Intelligent FMC Carrier AMC providing infrastructure for 2 High Pin Count (HPC) FPGA Mezzanine Cards (FMCs) and a RTM compliant to DESY D1.4 Class [7]. The card embeds a QorIQ T2081 PPC processor and a Xilinx Kintex Ultrascale XCKU040 (or XCKU060) FPGA [8]. This AMC has been developed as in-kind contribution from Paul Scherrer Institut (PSI) Switzerland by IOxOS Technologies. This card will be used by Beam Diagnostics, RF-LPS and Machine Protection. A picture of the card is presented in Fig. 2
- *SIS8300*: Struck AMC digitizer card with 10 channels 16-bit 125 Msps ADCs and 2 16-bit DACs and support for RTM cards compliant to DESY analog classes [9]. This card is used for Beam Diagnostics and LLRF systems.
- *IFC1420*: IOxOS high performance digitizer AMC with 10 16-bit ADC channels at 250 Msps and 4 16-bit DACs at 2.5 Gsps. The board embeds a QorIQ T2081 CPU, supports RTM cards compliant to DESY A1.1CO and has 1 HPC FMC slot [10]. This AMC has been developed as in-kind contribution from from PSI, Switzerland, by IOxOS Technologies. This card is designed to be a direct replacement for the SIS8300.
- *DWC8300*: DESY/Struck 10 channel downconverter RTM card compliant with DESY A1.1 Class.
- *DWC8VM1*: DESY/Struck 10 channel downconverter and vector modulator RTM card compliant with DESY A1.1 Class.
- *RTM Carrier*: low cost AMC card based on Xilinx Artix 7 FPGA, developed to provide support to D1.0 Class compatible RTMs. It is developed as in-kind contribution by National Centre for Nuclear Research Świerk (Poland). This card is part of the LLRF system.
- *Piezo Driver (RTM)*: Two channels piezo driver RTM card. The card will be compliant to DESY D1.0 class and is developed by Polish in-kind contributors from DMCS. This card is part of the LLRF system [11].
- *Local Oscillator and Clock Distribution (RTM)*: Local Oscillator and Clock generation and distribution RTM card for the 704.42MHz LLRF systems of ESS. The card will be compliant to DESY D1.0 class and is developed by Polish in-kind contributors from PEG [12].
- *ACQ420FMC*: d-tAcq Solutions FMC digitizer card with 4 channels 16-bit 2 Msps.
- *ADC3110/3111*: IOxOS FMC digitizer card with 8 channels 16-bit 250 Msps ADCs either AC (ADC3110) or DC (ADC3111) coupled.
- *ADC3112*: IOxOS FMC digitizer card with 4 channels 12-bit 900 Msps ADCs.
- *DAC3113*: IOxOS FMC with dual channel 16-bit 250 (500) Msps DAC and dual channel 16-bit 250 Msps ADC.
- *ADC3117*: IOxOS FMC digitizer card with 20 channels 16 bits 5 Msps ADCs. Designed on request by ESS. This FMC is used as building block for the RF-LPS system.
- *DIO3118*: IOxOS FMC digital IO card. Designed according to ESS specifications for the Fast Beam Interlock section of the RF-LPS.
- *FMC-Pico-1M4*: CAENels 4-channel 20-bit 1 Msps FMC Floating Ammeter card.
- *FMC-4SFP+*: CAENels FMC card with 4 SFP/SFP+ modules support.

Figure 2: IFC1410 Intelligent AMC FMC carrier.

Components Interconnections

As previously described the MicroTCA backplane provides a broad range of interconnections, either direct ones between two or more AMC cards or indirect by using the switching capabilities embedded in the MCH. These interconnections allow to reduce the amount of external cables.

PCIe purpose is to provide a channel for bulk data transfers between acquisition and CPU cards and to allow the latter to configure, control and monitor the overall status.

Ethernet link on AMC port 0 is used to provide network connectivity to CPU cards. These boards will retrieve the appropriate OS files and communicate with the control system through this interface.

Overall synchronization amongst the MicroTCA systems is provided by the timing system. The Event Receiver card recovers the 14 Hz machine clock from the data received by the Event Generator through an SFP optical module and distributes it through the backplane using the MCH clock module which is designed to receive and drive clocks from/to all TCLKA/B AMC ports. The EVR also provides trigger signals by means of the backplane M-LVDS lines.

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Remote Management

ESS aims to have an availability greater than 95%, in order to fulfil this requirement it is necessary to rely on redundant electronics for critical systems, whenever it is economically possible, and to a constant monitoring of the functional status. This will allow for an easy discovery and quick replacement of faulty electronic cards. ESS is currently at work to provide this monitoring capability to the EPICS layer either through an in-kind contribution or by an internal working group. The final goal of this project would be to create a scalable tool capable of interacting with virtually any number of connected systems and that will allow to:

- read FRU (MCH, PM, CU, AMCs, backplane) information and device ID;
- read and set activation (hot-swap) states;
- read sensors data record, values, including reading factors, and provide human readable values;
- set sensor threshold levels for alarms;
- read link capabilities and status;
- firmware update via HPM.1 .

System Startup

At the time of this writing two Operating Systems are supported, a customized CentOS based Linux distribution for x64 architectures and a NXP (formerly Freescale) Linux distribution for PowerPCs. ESS is currently adopting a diskless policy for booting up the AMC cards embedding a PPC. A server connected to the technical network will provide NFS and TFTP services to allow the bootloaders to retrieve the appropriate kernel images. In more details the PPC architecture boot procedure will rely on *"Das U-boot"*, an open-source bootloader, whose environment will be configured to retrieve, using TFTP protocol, a compiled script file for that specific machine based on its MAC address. The script file defines a list of settings that configure U-boot for the right TFTP and NFS exported files and folders. It will then load the appropriate kernel image, device tree blob and root file system for that machine. Pre-compiled EPICS Base and modules will be loaded using the same NFS service after the boot procedure [13].

CURRENT ESS STATUS

There are many systems currently under development or test for all the four categories previously mentioned. This section will focus on two relevant test stands that provide a good insight on the technology and on the platforms selected.

IFC1410 Testbench

This subsection will focus on the acquisition system that is currently under development at ICS, the Integrated Control System group of ESS, and at PSI (Switzerland) using the ESS official generic data acquisition platform, an AMC card provided as part of the in-kind agreement between the two institutes and developed by IOxOS Technologies. The test stand comprises the following MicroTCA infrastructure:

- 3U crate by Schroff;
- NAT-MCH-PHYS MTCA Carrier Hub by NAT;
- NAT-PM-AC600D 600W Power Module by NAT;

and the application specific cards:

- AM 900/412-99 CPU Board by Concurrent Technologies;
- MTCA EVR-300U Event Receiver by MRF;
- IFC1410 Intelligent FMC Carrier by IOxOS;
- ADC 3110 FMC digitizer card by IOxOS.

Figure 3 shows the system currently used as test stand.

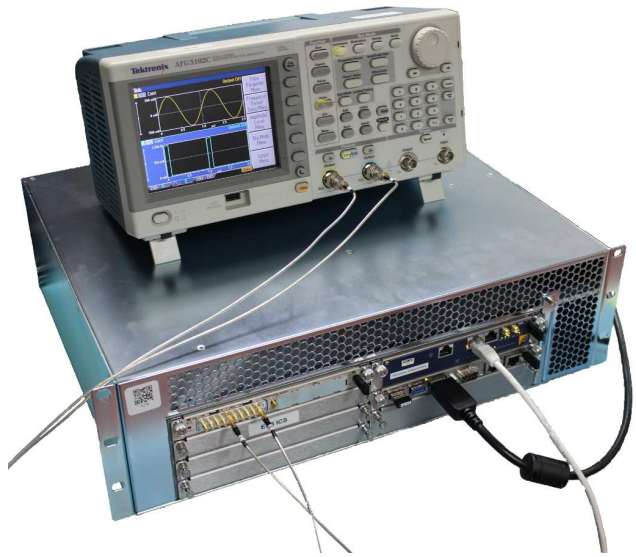

Figure 3: IFC1410 test stand w/o EVR.

The IFC1410 is an AMC FMC carrier card embedding two 7-series FPGAs from Xilinx, a low cost Artix-7 and a Kintex Ultrascale. The board also hosts a NXP QorIQ PPC CPU. The card is designed to provide the necessary infrastructure for 2 High Pin Count FPGA Mezzanine Cards (FMCs). The Artix-7 is used to manage the start-up sequence and configuration of the board, it provides the appropriate bitstream to the Kintex Ultrascale central FPGA, either directly or by interaction with the PPC, and interfaces with the Module Management Controller (MMC). Figure 4 shows an overview of the available components and interconnections provided.

The FPGA is directly connected to 2 independent 512MBytes DDR3L memory blocks that are used as buffers for the incoming data from the FMCs. The PowerPC is connected to 2 GBytes of DDR3L ram and runs a custom made Linux distribution based on the latest available NXP QorIQ SDK. The two-fold role of the CPU is as follows:

- it interacts with the PON FPGA at start-up. It retrieves the Central FPGA bitstream from the remote TFTP server;
- it executes the EPICS IOC that provides information to the control system.

The PPC directly connects to the MicroTCA backplane Gigabit Ethernet interface and can access the external technical network through the Ethernet switch embedded in the MCH.

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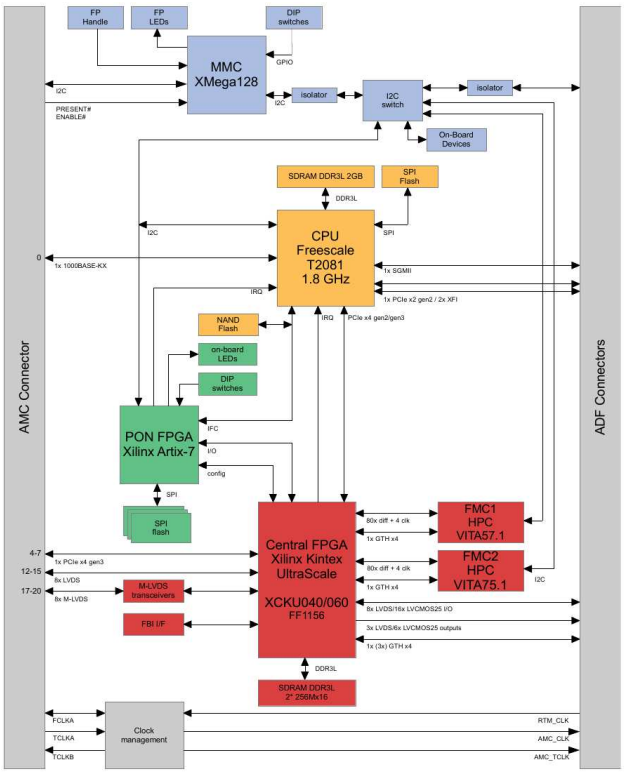

Figure 4: IFC1410 block diagram [14].

The FPGA firmware is based on the IOxOS proprietary Network on Chip (NoC) architecture called Tosca [15]. The currently available revision of the framework is the Tosca IIb and consists of the VHDL implementation of a full mesh switch for bulk data transfer and a common shared bus interface to control the available IO resources and manage the events/interrupts. Tosca IIb offers individual paths for data requests and responses between the different "*entry points*", called Agent Switches (AS).

The interconnections are implemented with 64 + 8 bit paths running at 250 MHz and the data packets use a header whose architecture closely follows the one used for PCIe Transaction Layer Packets (TLP). Out of the 8 AS interfaces provided by the hardware vendor two are dedicated to the PCIe interfaces towards the MicroTCA backplane and the on-board T2081 PPC CPU, two connects to the DDR3L memory blocks, one is connected to the transceivers routed to the Zone3 interface (connection to the RTM), one is reserved for future implementation of an AXI compliant bus interface and two are used for user specific implementations. The current firmware design uses the user reserved AS to connect a Scope Application collecting data from the ADC 3110 FMC card [14]. The VHDL code was modified in order to receive incoming trigger signals from the backplane M-LVDS lines.

This system offers a great degree of flexibility, by replacing the FMC cards installed on the carrier many applications can be covered. The RF Local Protection System for instance will rely on an IFC1410 equipped with one ADC3117 20-channel digitizer mezzanine card and one DIO3118 FMC that receives and transmits digital signals.

LLRF Testbench

The development of the ESS LLRF system is coordinated by the Lund Technical University (LTH) and involves in-kind contributions from the member institutes of the Polish Electronic Group (PEG) which are the National Centre for Nuclear Research (NCBJ), the Warsaw University of Technology (WUT) and the Technical University of Łódź (TUL). LTH and ESS are responsible for the development of the digital control algorithm, firmware implementation and EPICS integration while the PEG will deliver the AMC and RTM cards to control the RF cavity piezoelectric tuners and generate and distribute the LO and ADC Clock signals to the acquisition card.

The test stand for this system currently comprises the basic infrastructure components:

- 9U crate by Schroff;
- NAT-MCH-PHYS MTCA Carrier Hub by NAT;
- MTCA 4.0 1000W PS Power Module by WIENER;

and the application specific cards:

- AM 900/412-99 CPU Board by Concurrent Technologies;
- MTCA EVR-300U Event Receiver by MRF;
- SIS8300 digitizer card by Struck;
- DWC8VM1 10 channel down-converter and vector modulator RTM card by DESY/Struck.

Figure 5 represents an overview of the system.

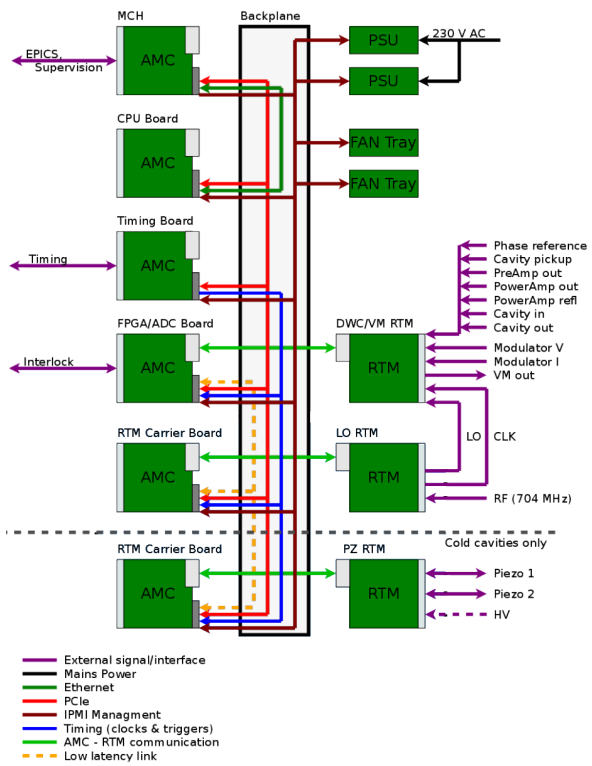

Figure 5: General layout of single ESS LLRF unit [16].

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At the time of this writing the control algorithm and the analog to digital conversion of the incoming signals are performed using a Struck SIS8300-L2 AMC card connected to the DWC8VM1 RTM. An Intel i7 based CPU card is responsible for configuring the digitizer board, setting the controller parameters, evaluate correction tables at run time and to interface the system to EPICS. The digitizer card embeds a Xilinx Virtex VI FPGA that interfaces on the backplane by means of 4 PCIe lanes and 2 GbE connections. Additional transceivers are used to provide two external SFP modules and four AMC to AMC connections on the backplane ports 12 to 15. The AMC is also designed to receive trigger signals on the M-LVDS backplane lanes. The board is equipped with 2GB DDR3 memory that directly interfaces to the FPGA. ADC and DAC clocks can be derived either from the front panel connectors on the AMC and RTM cards or from the backplane or from an internal oscillator. The SIS8300 provides 10 16-bit ADC channels sampling at up to 125Msps and two 16-bit DAC channels running at 250Msps. The LLRF firmware is currently implemented on top of Struck proprietary framework but provisions are made to create a new BSP based on Xilinx IPs interconnected using AXI bus for the newly released KU version of the AMC card [17, 18].

Discussions are ongoing to replace the SIS8300 digitizer card with the IFC1420 AMC that is going to be provided by PSI as part of the current in-kind collaboration. This card is designed to be a direct hardware replacement for the SIS8300 in the sense that it provides a Zone 3 connector pinout that complies to DESY A1.1CO and thus supports the same RTM boards. The IFC1420 design is derived from the IFC1410 and like its predecessor it includes the T2081 PPC CPU with 2GB dedicated DDR3L memory and the same PON and Central FPGAs. The Kintex Ultrascale FPGA directly connects to the 2 512MB DDR3L Memory blocks and interfaces to the available HPC FMC slot and to the ADC and DAC sections. The analog to digital and digital to analog circuitries are part of a removable daughter card, this mezzanine module does not comply to any mechanical specification, nevertheless it uses a standard FMC connector to route the digital interfaces and a specialized one for the analog signals. This solution offers the flexibility to change the sampling rate performances without the need to redesign the control section on the AMC. The digital interfaces towards the ADCs are kept as similar as possible to those provided in comparable FMC cards thus easing the porting of the HDL code. The additional FMC slot can be used to interface to other external systems like the Machine Protection one. The first prototype of this card will provide a converters section with 10 16-bit ADC channels up to 250Msps and 4 16-bit DAC channels at 2.5 Gsps [19]. The input stage of the ADCs can be factory configured to be AC or DC coupled. This AMC, like the IFC1410, provides the following connections on the backplane:

- Gigabit Ethernet links on ports 0 and 1 are connected to the PPC;
- PCIe x4 Gen3 link between ports 4 to 7 and the Central FPGA;
- Point-to-point M-LVDS lines controlled by the FPGA on ports 12 to 15;
- Bus M-LVDS links controlled by FPGA on ports 17 to 20;
- Clock received on TCLKA and distributed on TCLKB.

Additional input clocks are provided by the RTM interface. The firmware infrastructure will be based, like for the IFC1410, on the IOxOS proprietary Tosca NoC.

SUMMARY AND OUTLOOK

ESS project relies on many in-kind contributions from institutes of member nations, this is reflected in the choice of hardware to be used to implement the many monitor and control systems. A new set of AMC and RTM cards have been developed or are currently under development to cover all ESS requirements. Two variants of a single board computer AMC have been manufactured and provided as result of the in-kind collaboration with PSI, these card are tailored for data acquisition systems and can be customized for different applications by selecting from the broad list of COTS FMC cards available on the market. The integration of the NXP QorIQ PPC CPU on the same AMC card offers the flexibility of running separate EPICS IOCs on each acquisition card. The lack of PCIe connectivity on the MicroTCA backplane for the PPC limits the usability of the card as an *upstream* device on the FAT Pipe Region which implies that the management of other AMC *end-point* boards still requires an additional, conventional, CPU card installed in the chassis. At the time of this paper discussions are on-going on how to improve the current design to allow this cards to be used as the controller of the system for those applications where a low performance CPU might suffice. This will decrease the overall system cost and reduce the chassis slot consumption.

REFERENCES

[1] *"PICMG 3.0 Revision 3.0 - AdvancedTCA Base Specification"*, PICMG, 401 Edgewater Place, Suite 600 Wakefield, MA 01880, USA.

[2] *"PICMG Specification MTCA.0 R1.0 - Micro Telecommunications Computing Architecture Base Specifications"*, PICMG, 401 Edgewater Place, Suite 600 Wakefield, MA 01880, USA.

[3] *"PICMG AMC.0 R2.0 - Advanced Mezzanine Card Base Specification"*, PICMG, 401 Edgewater Place, Suite 600 Wakefield, MA 01880, USA.

[4] ESS, `https://europeanspallationsource.se/technology`, URL date Sep. 2017.

[5] J. Cereijo Garcia, J. H. Lee, and T. Korhonen, *"Timing System at ESS"*, presented at the 16th Int. Conf. on Accelerator and Large Experimental Physics Control Systems (ICALEPCS'17), Barcelona, Spain, paper TUPHA088, this conference.

[6] Pentair Schroff, *"3U MTCA.4 Shelf 6 Slots"*, Langenalber Strasse 96-100, D-75334 Straubenhardt, Germany.

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUAPL01

[7] *"Zone 3 Connector Pin Assignment Recommendation for Digital Applications for AMC/μRTM Boards in the MTCA.4 standard"*, http://mtca.desy.de/sites/site_mtca/content/e174425/e199301/e199408/ZONE_3_Classification_Recomendation_Class_D1.0-4_RevA.3_eng.pdf, Mar. 2013.

[8] IOxOS Technologies, *"IFC1410_HW_UG"*, CH-1196, Gland, Switzerland.

[9] *"Zone 3 Pin Assignment Recommendation for Analog Applications for AMC/RTM Boards in the MicroTCA.4 standard"*, https://mtca.desy.de/sites/site_mtca/content/e174425/e199301/e243879/e243880/ZONE_3_Classification_Recomendation_Class_A1_RevA.4_eng.pdf, Aug. 2014.

[10] IOxOS Technologies, *IFC_1420 MTCA.4 Fast Digitizer AMC Conceptual Design"*, unpublished.

[11] D. Makowski, A. Mielczarek, G. Jabłoński, and P. Perek, "Preliminary Design Report for Piezo Control Device", ESS, Lund, Sweden, PDRs of LLRF parts, May 2017.

[12] I. Rutkowski, "LO RTM Design Report", ESS, Lund, Sweden, PDRs of LLRF parts, May 2017.

[13] J. P. S. Martins, S. Farina, J. H. Lee, and D. Piso, "MicroTCA.4 integration at ESS: from the front-end electronics to the EPICS OPI", presented at the 16th Int. Conf. on Accelerator and Large Experimental Physics Control Systems (ICALEPCS'17), Barcelona, Spain, paper THPHA133, this conference.

[14] IOxOS Technologies, *"IFC_1211/IFC_1410 XUSER User's Guide"*, CH-1196, Gland, Switzerland.

[15] J. Bovier, P. Cristin, and J. F. Gilot, *"TOSCA II User's Guide Architecture"*, IOxOS Technologies internal manual, 2011.

[16] J. Szewiński and M. Gosk, "Preliminary Design Report for the RTM Carrier", ESS, Lund, Sweden, PDRs of LLRF parts, May 2017.

[17] A. J. Johansson, "LLRF system description", ESS, Lund, Sweden, PDRs of LLRF parts, May 2017.

[18] M. Kirsch, "Kintex Ultrascale based MTCA digitizer cards, the SIS8300-KU and beyond", lecture given at 5th MicroTCA workshop for industry and research, Hamburg, Germany, Dec. 2016.

[19] IOxOS Technologies, *"DAQ_1430 ADC/DAC MEZZANINE BOARD"*, unpublished.