LCLS-II TIMING PATTERN GENERATOR CONFIGURATION GUIs*

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Abstract

The LINAC Coherent Light Source II (LCLS-II) is an upgrade of the SLAC National Accelerator Laboratory LCLS facility to a superconducting LINAC with multiple destinations at different power levels. The challenge in delivering timing to a superconducting LINAC is dictated by the stability requirements for the beam power and beam rate up to 1MHz (Table 1). A timing generator will produce patterns instead of events because of the large number of event codes required. This paper explains how the stability requirements are addressed by the design of two Graphical User Interfaces (GUI). The Allow Table GUI filters the timing pattern requests respecting the Machine Protection System (MPS) defined Power Class and the electron beam dump capacities. The Timing Pattern Generator (TPG) programs Sequence Engines to deliver the beam rate configuration requested by the user. The TPG generates the patterns, which contain the timing information propagated to the Timing Pattern Receiver (TPR). TPG and TPR are implemented in FPGA solution and configured at the EPICS level. This paper will explain the requirements and show an overall design of the high-level software solutions that meet the physics requirements for LCLS-II timing.

INTRODUCTION

LCLS-II timing system does a variety of tasks for the triggering and synchronizing of the beam bunches and data acquisition. The configuration of the timing system can be accomplished on a low-level programming or by a user-friendly interface. The timing GUIs will be generating beam rate patterns including all the intermediate rates between 0 and CW operation at 1MHz. The GUIs will also allow the generation of single shot and burst mode. The timing team, together with the physicists and the MPS team, identified three GUIs to meet specifications; the identified interfaces are listed in Figure 1.
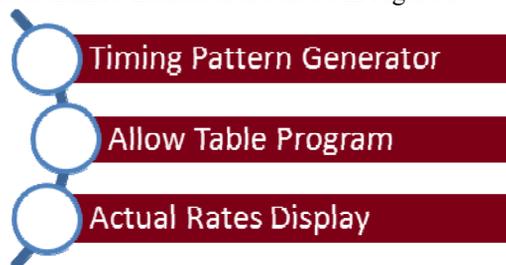
Figure 1: TPG GUIs list.

This paper will describe the features offered by each one of the listed GUIs.

BEAM RATE PATTERN

The LCLS-II Timing System prescribes the actions to be performed on a sequence of bunches as they are injected into the accelerator using the timing pattern. The timing pattern will dictate the rate, temporal separation of bunches and the bunch destination (to the HXR, SXR, dumps etc.) as well as other parameters that can be altered on a bunch-by-bunch basis (energy, peak current etc.). The pattern that is applied to the sequence of bunches will repeat itself continuously until the timing generator makes a change in the pattern [1].

There are two classes of beam rate pattern: Standard beam rate and the AC synchronous beam rates.

Standard Beam Rate Pattern

The standard patterns are defined as a fixed integer number of RF phase reference cycle.

The LCLS-II standard patterns are listed in Table 1.

Table 1: LCLS-II Standard Pattern Rates

Nominal Rate	Exact Rate
Zero rate	0
Single shot	Once, on request
Burst mode	Specify number of shots
	Specify number of spacing
1 Hz	0.928 Hz
10 Hz	9.28 Hz
50 Hz	46.4 Hz
100 Hz	92.8 Hz
1 kHz	0.928 kHz
10 kHz	9.28 kHz
100 kHz	92.8 kHz
Half rate	262.285 kHz
Full rate	928,571,428.571 Hz

The described patterns are absolute and not locked to the variable AC frequency [1].

AC Synchronous Beam Rates

The beam rates included in this class are locked to the AC power line. In spite of the standard pattern rates, the AC synchronous beam rates do not guarantee the same number of RF cycle at full rate.

The following list contains the beam event triggers synchronized to the power line:

- Time slot assignment for AC synchronous beam rate;
- Bunch trains;
- Bunch trains to compensate beam-loading transients.

The format of the timing pattern frame is enumerated in Table 2. (Figure 2)

TUMPL04

Table 2: Timing Pattern Frame

Field	Size	Description
Pulse ID	64	Unique, monotonic., increments at base rate
Time Stamp	64	Time since 1990 epoch., increments at programmed step size
Fixed Rates	10	Fixed rate markers 0-9;one bit for each
ACRates	6	Power line synchronized markers 0-5, one bit for each
Time Slot	3	360Hz time 1-6 persistent. Computed from TS1 input
Beam Request	1	Beam is requested from the injector
Destination	4	Beam destinations
Charge Inj.	16	Bunch charge
Beam Energy	4x16	Beam energy at 4 locations
BSA Control	4x64	For each buffer, initialize, average, acquire, finalize
ControlSeq[0:17]	288	16b control step data for each of 18 sequences
+others		
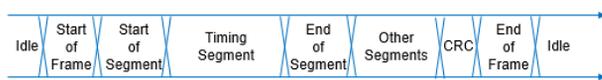
Figure 2: Timing pattern frame (visual).

The timing pattern frame itself is encapsulated within control characters that allow additional data streams to be serialized onto the link. This configuration allows transmission of differing domains that firmware outside of that domain are not required to parse. The entire 1MHz frame is validated by 32-bit CRC calculation.

Beam pattern generation, together with MPS rate reduction setup, and sequenced triggering are instructions executed by the 50 instruction processor engines in firmware. Each processing engine has 2048 instruction cache and loop up to four level depth [2].

All the processing engines are programmed via the same EPICS interface: the timing generator high-level applications.

TIMING PATTERN GENERATOR

The Timing Pattern Generator GUIs (TPGGUI) uses the EPICS PVs provided by the TPG IOC to program the Sequence Engines at the FPGA level. The Physics requirements document describes the desired functionalities for the timing configuration. There are multiple challenges hard to address at 1MHz, as Multiple Destinations and Bunch Trains. LCLS-II phases of commissioning (Early Injector Commissioning and Production Commissioning)

with the requirement to configure bunch trains expressed the need to have three level of customization for the TPG GUI design:

a) Parameterize configuration (Figure 3)
b) Manual bunch entry configuration (Figure 4)
c) pre-configured sequences selection (Figure 5)

### TPG GUI Parameterize configuration
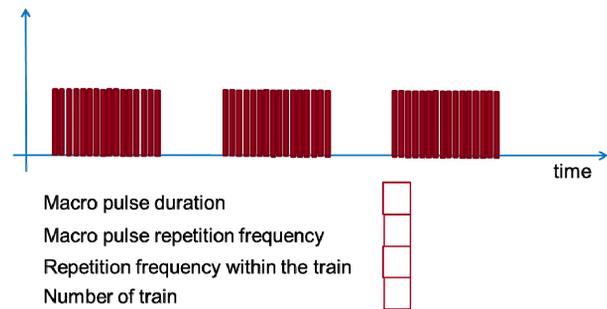
Figure 3: TPG GUI parameterize (smaller trains and fixed spacing).

Programming bunch trains is more effective when the GUI allows the users to enter parameters to define the number of macro pulse duration, macro pulse repetition's frequency, repetition frequency within the train and the number of trains to repeat the bunch train configuration.

This GUI will be available for LCLS-II production commissioning together with the manual bunch entry configuration GUI. This GUI allows easy configuration of parameterized bunch trains to run at 1 MHz.

### TPG GUI Manual Bunch Entry Configuration

Figure 4: TPG GUI manual bunch entry configuration.

The initial design of the TPG GUI allows the user to manually configure each bunch.

This interface design allows the user to store or retrieve commonly used beam patterns and to compose new sequences. The full implementation of this GUI will program the beam pattern requests to all destinations including diagnostic lines and dumps. It also responds to the MPS rate reduction requests. The implementation of MPS requested rate reduction is addressed by the Allow Tables.

The TPG GUI Manual bunch entry configuration offers the following options for the user:

1. create a bunch train
2. modify or make a new "rate name" based on an existing one
3. delete a "rate name"
4. install timing sequences.

As shown in Figure 4, option 2 does satisfies physics requirements; the user can select a bunch and assign to it a charge, rate marker and a destination [2]. The destination's power count increases when bunches are assigned to it, in order to always respect the destination capacity. The slider allows movement along the bunch train to select and configure each bunch.

TPG GUI Pre-configured Sequence Selection

During Early Injector Commissioning (EIC), the patterns will be limited to trivial implementations of fixed rate beam patterns to one destination. This is possible because the timing system requirements for generating timing patterns for EIC are reduced:

- Limited set of beam rates
- max charge limited to 300pC
- one destination (GUN B)
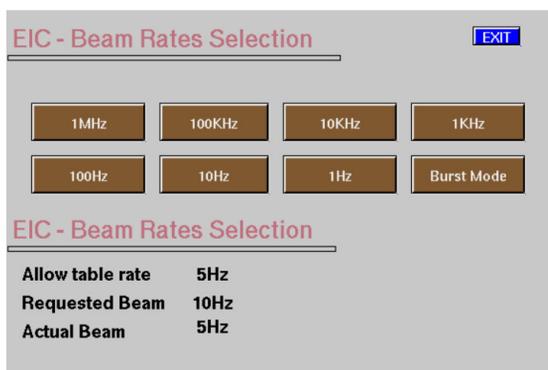
Figure 5: TPG GUI manual bunch entry configuration.

ALLOW TABLE PROGRAM

The MPS system uses the timing system as a mitigation device to reduce rate.

Definitions:

- *Power Limit (PL):* This is the maximum power authorized from MPS, communicated by the Central Node.
- *Allow Sequence (AS):* This is the set of timing sequences allowed for a specific Power Class (PC).

The communication between the Timing System and MPS is fundamental to calculate the Allow Table. The GUI program receives input from MPS about rate reduction requests. The rate reduction request is communicated via the MPS's Central Node to the Timing Generator, Figure 6. Once the allowed Power Limit is communicated, the *Allow table program GUI* selects a sub set of allow sequences.
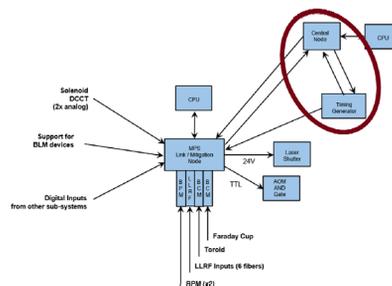

Figure 6: MPS communication with the Timing System.

The TPG GUI has a table of all the timing sequences and the charge associated with each configuration. The program filters from this table all the sequences that match MPS's charge requirement. The filtered timing sequences, called "Allow Sequences", represent the common sets of "Allow Tables". The user beam request can be extracted from these, allow tables and pre-allocate beam buckets for minimal setup changes.

The Timing system is also communicating to the MPS, the desired charge. When the user defines the timing sequences, desired charge is selected. The desired charge is important information for MPS, to use for comparing the actual measured charge in order to take preventive actions if required.

Early Injector Commissioning

The requirements for EIC are reduced, with a maximum charge of 300pC. A fixed maximum charge permits a static allow table as shown in Figure 7.

Figure 7: Allow Table Interface design.

ACTUAL RATE DISPLAY

The "Actual Beam" rate may differ from the "Requested Beam" rate if higher than the "Allow table rate".

For EIC the control room is going to use a unique display with the rates selection that includes the "Actual Rate" and the "Desired Rate" for the one destination, Figure 8.

For Commissioning, a display will be developed to support machine operation. The "Actual Rate" is compared to "Desired Rate" for all destinations: Diagnostic Line, D10, SXR and HXR. This display has a very clear and simple design that allows Operation to identify when the actual rate is lowered by MPS or requires further troubleshooting.

Figure 8: Actual Rate Display for EIC.

CONCLUSION

The Timing System GUI designs are required by the system to be very flexible.

The user interfaces have the appropriate level of complexity. Early Injector Commissioning requirements are reduced allowing a simplified version of the GUIs. The complexity increases when the interfaces have to satisfy LCLS-II machine commissioning.

The programs and GUIs are designed and developed to generate patterns that dynamically adapt to what MPS allows for the current condition. The GUIs described in this poster provide the timing interface for use with multiple systems. The user interfaces are designed to be friendly and intuitive.

ACKNOWLEDGEMENT

REFERENCES

[1] *Timing System Physics Requirements Document*
https://docs.slac.stanford.edu/sites/pub/Publications/Timing_System_PRD.pdf

[2] *LCLS-II Timing System Engineering Specifications*
https://docs.slac.stanford.edu/sites/pub/Publications/LCLS-II_Timing_System_Engineering_Specifications.pdf