ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA032

PARALLEL PROCESSING FOR THE HIGH FRAME RATE UPGRADE OF THE LHC SYNCHROTRON RADIATION TELESCOPE

D. Alves*, E. Bravin, G. Trad, CERN, Geneva, Switzerland

Abstract

The Beam Synchrotron Radiation Telescope (BSRT) is routinely used for estimating the transverse beam size, profile and emittance in the LHC; quantities playing a crucial role in the optimisation of the luminosity levels required by the experiments. During the 2017 LHC run, the intensified analog cameras used by this system to image the beam have been replaced by GigE digital cameras coupled to image intensifiers. Preliminary tests revealed that the typically used sub-image rectangles of 128×128 pixels can be acquired at rates of up to 400 frames per second, more than 10 times faster than the previous acquisition rate. To address the increase in CPU workload for the image processing, new VME CPU cards (Intel 4 core/2.5GHz/8GB RAM) are envisaged to be installed (replacing the previous Intel Core 2 Duo/1.5GHz/1GB RAM). This paper focuses on the software changes proposed in order to take advantage of the multi-core capabilities of the new CPU for parallel computations. It will describe how beam profile calculations can be pipe-lined through a pool of threads while ensuring that the CPU keeps up with the increased data rate. To conclude, an analysis of the system performance will be presented.

THE BSRT INSTRUMENT IN THE LHC

The BSRT (Beam Synchrotron Radiation Telescope) is a very important instrument for the operation of the LHC and is currently the only system providing non-invasive measurements of the transverse beam size for calculation of emittance on a per-bunch basis. It does so by imaging the light intensity of visible and ultra-violet synchrotron radiation produced by the particles in each bunch.

Synchrotron radiation is generated whenever the trajectory of a moving, charged particle is bent due to a magnetic field. This radiation is emitted in the forward direction, in a narrow cone tangentially to the trajectory. The emitted radiation power is proportional to the fourth power of the beam energy and inversely proportional to the square of the bending radius.

In the particular case of the LHC, where the beam energy currently lies between $450GeV$ and $6.5TeV$, one can see that the BSRT system is required to handle a change of more than 4 orders of magnitude in terms of radiation power. For this reason, the BSRT setup comprises a set of optical filters placed between the light source and the image intensifier, to keep the light intensity in a range where it will not damage either the camera or the image intensifier. A simplified diagram of the instrument setup is shown in Fig. 1. In this diagram, most of the complexity of the overall setup including the details of the optical telescope path, light splitters, lenses etc have been omitted. For more details see [1].

HARDWARE OVERVIEW

The hardware setup comprises various items. On the instrument side itself, a subset of the components requiring real-time control are:

- **Digital camera** - Basler Ace area scan CMOS-based 1936×1216 resolution camera
- **Relays** - controls camera on/off state
- **Image intensifier** - enhances/controls light intensity seen by the camera
- **Relays** - controls on/off state of image intensifier
- **Pneumatic device** - control of combinations of optical filters
- **3x step motors** - x,y,z position control of the camera
- **2x step motors** - x,y position control of the image steering mirror

The major change for the BSRT between the 2016 and 2017 LHC run was the replacement of the original analog cameras with digital cameras. The new cameras, Basler ACE acA1920-50gm [2], are CMOS-based cameras with 1936×1216 pixel resolution and a 1Gbit/s ethernet interface. Preliminary tests have shown that, when configured in free running mode and in steady state conditions, 128×128 pixels (typically used in LHC operations) can be streamed over ethernet at rates close to 400 frames/sec. Another crucial component of the overall system is the image intensifier which consists of a photo-cathode, a multi-channel-plate electron amplification stage and a fluorescent screen for enhancing the intensity of the light seen by the cameras. The connection between these components and their power supplies is controlled via relays using a serial interface. Such devices are also used to control the different optical filter combinations required to obtain the desired light attenuation. Finally, various stepping motors are used in real-time to control both the position of the camera and the image steering mirror to ensure the beam spot is always centred.

The VME-based [3] hardware used for the control, data acquisition and real-time processing of the BSRT instrument comprises the following modules:

- **CPU1** - runs the BSRT main controller as well as the controllers for the pneumatic actuators and relays
- **CPU2** - runs the stepping motor controllers

* diogo.alves@cern.ch

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA032

- **BOBR** - timing card that receives the LHC turn and bunch clock required for synchronising the system with the various bunches in the machine
- **STTY** - serial interface card
- **DAB** - general purpose FPGA motherboard used for triggering the bunch gating and the camera acquisition
- **VMOD** - general purpose board supporting mezzanines for analog and digital I/O
- **STEPCTRL** - control of the stepping motors

Two VME crates are presently used for the online BSRT system. The VME compatible MEN-A20 CPU boards [4] employ an Intel Core 2 Duo (dual core) processor with a clock frequency of 1.5GHz per core and 1GB of RAM. The (Beam Synchronous Timing Receiver) BOBR card [5] is used to receive the synchronous LHC turn and bunch clock required for gating the camera images on each bunch. The Data Acquisition Board (DAB) [6] is a custom made CERN generic card designed by TRIUMF (Canada) with on-board digital signal processing capabilities. This is used for sending the gating signal to the image intensifier and for providing the hardware trigger for the camera. The VMOD, a general purpose card supporting mezzanines for analog and digital I/O, is mainly used in this system for driving the gain of the image intensifier (analog) and configuring the camera triggering mode (TTL).

As depicted in Fig. 1, the synchrotron radiation emitted is channeled through an optical telescope assembly towards a mirror that steers the light through an appropriate set of attenuation filters to the image intensifier from which light is generated for the CMOS sensor of the camera. Both the mirror and the camera are mounted on moveable stages which are controlled in real-time via stepping motors using the in-house developed STEPCTRL card. CPU1, which runs the main BSRT controller, directly uses the VME bus to control the bunch gating, camera triggering and intensifier gain via the various VME cards installed in the same crate. It also controls the camera on/off status and optical filter combinations via a serial interface (STTY card). As for CPU2, it runs the controller for the various stepping motors. The camera configuration and control is done via ethernet with the frames also streamed from the camera to the main BSRT controller application via ethernet.

CONTROL AND ACQUISITION SOFTWARE OVERVIEW

The control and data acquisition software running on the CPUs described in the previous section has been developed using the CERN Front-End Software Architecture (FESA) [7] C++ framework for real-time systems. This framework provides not only highly customisable multi-threaded scheduling facilities but also a tight integration the CERN control infrastructure including interfacing with

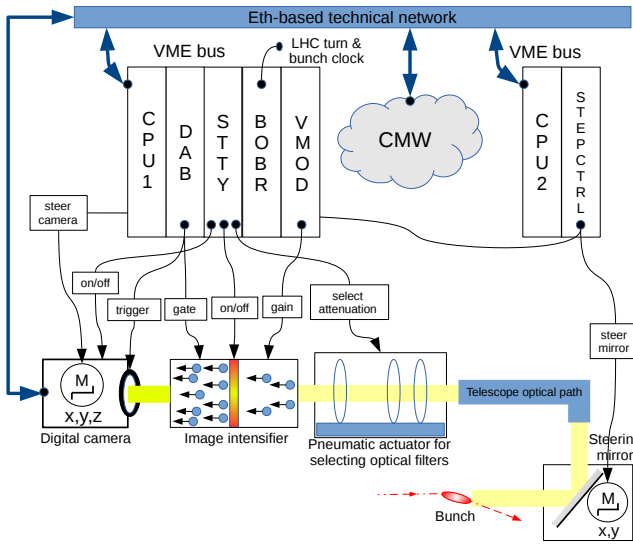

Figure 1: BSRT hardware overview.

the central timing system, data publishing and data subscriptions, data logging and message logging.

The BSRT main controller, the controller of the pneumatic devices and the controller of the BOBR card are all FESA-based processes running on CPU1 whereas the controller process for the stepping motors runs on CPU2, in a different VME crate. The data publishing/subscription scheme is provided by the Controls Middle-Ware (CMW) [8] tier which centrally manages the real-time sharing of data between systems using the CERN remote data access protocol. The real-time communication between the BSRT main controller process, the pneumatic device controller and the stepping motor controller is done via CMW.

The ethernet-based interface with the digital camera is provided using the Pylon5 [9] software library delivered by the manufacturer. The BSRT main controller process uses this library to configure the camera trigger mode (hardware trigger in this case), the region of interest, the integration time, the image binning, the image orientation and the camera gain. Control of these settings is performed at a rate of approximately $1Hz$, the same rate at which results are published. The image acquisition and processing loop is closely related to both the camera's integration time and the time spent processing the camera data. An example of an acquired frame together with a plot of its vertical projection and Gaussian fit is shown in Fig. 2.

IMAGE PROCESSING SCHEMES

In order to extract the average transverse beam sizes and calculate emittances, on a bunch-by-bunch basis, the acquired images have to be processed in real-time.

The scheme presently implemented in the online system is depicted in Fig. 3. For every bunch the gating has to be set so that the camera integrates the light coming strictly from that bunch. This is achieved by activating the intensifier only during the passage of the specified bunch every LHC turn (at

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA032

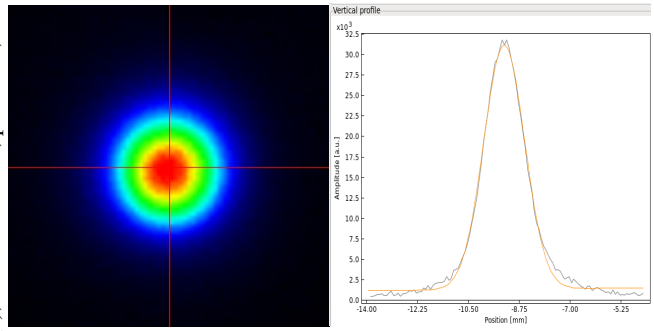

Figure 2: BSRT image, projection profile and fit example.

a rate of $11.2kHz$, the revolution frequency) while the camera is continuously integrating. The intensifier gain, which is calculated on a per-bunch basis and depends on the bunch intensity as well as the beam energy, is subsequently set before the camera is triggered. This is a fairly delicate step as excessive light intensity can damage the camera. Once complete, the camera is finally triggered to start integrating the input light. In the meantime, while the camera is integrating, if a previously acquired frame is available, the routines performing the X and Y image projections and the Gaussian fits are sequentially executed. Once the fits are complete, the freshly acquired frame is stored, its X and Y projections are calculated and stored along with the results of the previous fits. Based on the latest data the bunch gain is updated and a check is performed on whether the desired number of images per bunch has been acquired. If complete, then the active bunch is to be set to the next bunch and the whole process is repeated. Otherwise the process is repeated keeping the same bunch gating configuration. This is basically a single-threaded processing scheme which tries to make best use of the camera integration time to perform the Gaussian fits. Prior to the 2017 LHC run, when still using analog cameras, the integration time was set to $20ms$, the frame repetition rate was $25Hz$ and the number of required images per bunch was set to 5 in order to increase the signal-to-noise ratio. These translated into a scan rate of about 5-6 bunches per second, i.e. taking $8min$ to scan the nearly 3000 bunches circulating.

Already anticipating the foreseen installation of new processor boards with 4 cores [10], a new processing scheme has been benchmarked in the laboratory while still using the current CPUs. At the heart of this new processing scheme (see Fig. 4) is the concept of a *Thread Pair*. The idea behind *Thread Pairs* is to be able to parallelise the *orthogonal* X and Y operations, including the fitting. The other change between this and the previously described scheme is that, as soon as a thread pair is available and unleashed to start processing a freshly acquired image, the next image can start being acquired right away. It is clear that, with the presently available 2 core CPUs the main gain is in the parallelisation of the X and Y processing, however, as soon as more cores become available, the gain in processing time will increase even further.

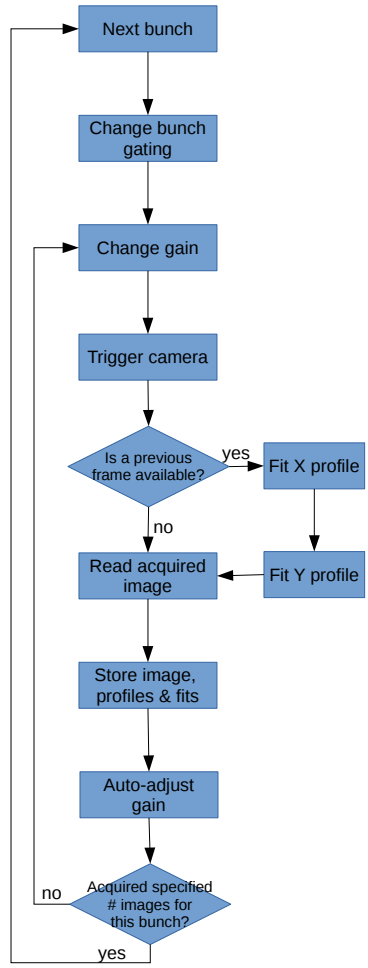

Figure 3: Data-flow diagram for the presently used image processing scheme.

Benchmarking tests of the method presently implemented online (described in Fig. 3 but acquiring only 1 frame per bunch rather than 5) and the newly proposed method with parallel fitting (described in Fig. 4) have been performed in a laboratory environment.

One can see, in Fig. 5 how the number of scanned bunches per second changes as a function of the camera integration time for each of these 2 methods when acquiring a single frame per bunch. An improvement of the newly proposed method over the present scheme can be observed. This improvement becomes more evident as the camera integration time decreases to values comparable to the average time taken by the Gaussian optimisation procedures (approximately $3 - 3.5ms$ per axis).

CONCLUSIONS

With this work we have demonstrated that the bunch scanning speed when using parallel processing to provide average transverse bunch sizes and emittances should be superior to the currently used technique. It can be seen for example, that for an integration time of $5ms$ there is an 18% (i.e. 14 bunch/sec) gain in terms of scanning speed by us-

ISBN: 978-3-95450-193-9 doi:10.18429/JACoW-ICALEPCS2017-TUPHA032

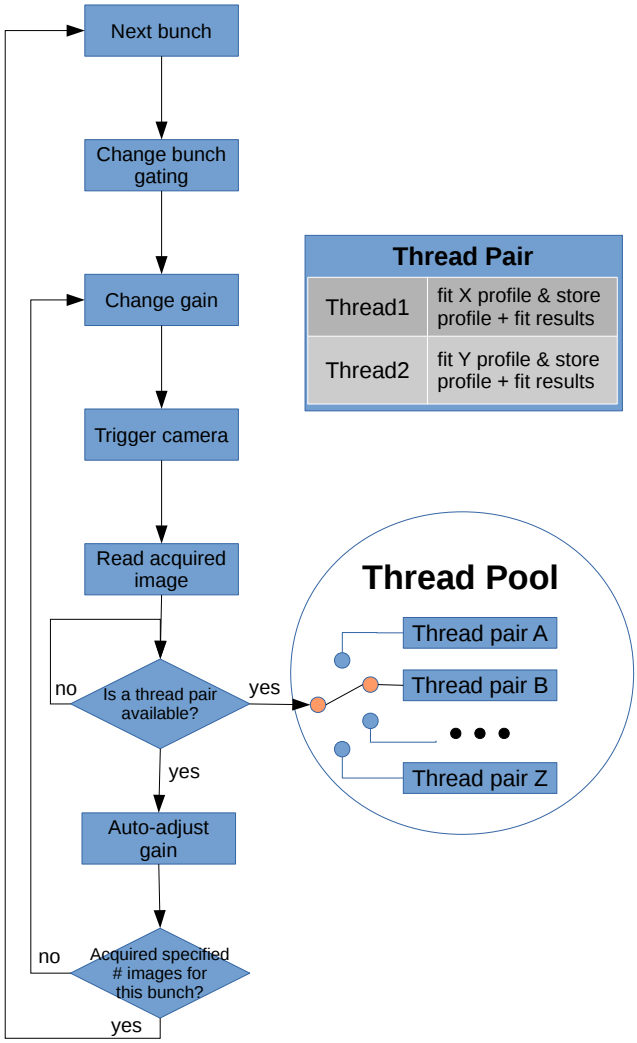

Figure 4: Data-flow diagram for the newly proposed image processing scheme.

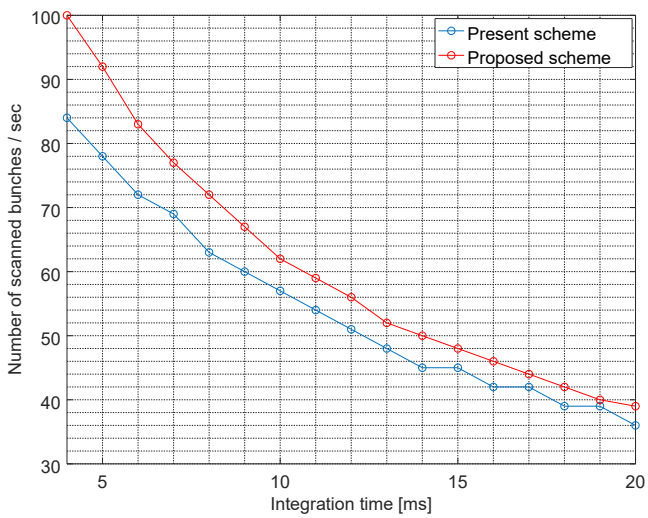

Figure 5: Bunch scanning performance.

ing the proposed parallel scheme. Although already quite relevant for current LHC operation, the main goal of this work is not to demonstrate that a performance gain could be achieved but to devise a scheme that would remain valid and scalable with the number of available cores. The extrapolation of the results of this test for the future MEN-A25 4 core processor card (using 2 *Thread Pairs*) is not straightforward since processor idiosyncrasies affecting performance are not simple to anticipate. However, from this test one expects that the gain in bunch scanning speed will only be evident for short integration times. Although short integration times mean less light hence a poorer signal-to-noise ratio, preliminary tests indicate that with the new digital cameras, and even for integration times of only a few milliseconds, the signal-to-noise ratio is good enough to perform the Gaussian fits and extract the transverse beam sizes.

ACKNOWLEDGEMENT

The main author would like to gratefully acknowledge the clarifications provided by A. G. Ollacarizqueta and S. B. Pedersen and the comments of S. Jackson.

REFERENCES

[1] A. Goldblatt, E. Bravin, F. Roncarolo, and G. Trad, "Design and Performance of the Upgraded LHC Synchrotron Light Monitor", in *Proc. 2nd International Beam Instrumentation Conference (IBIC'13)*, Oxford, UK, Sep. 2013, paper MOPF08, pp. 220–223.

[2] Basler Ace Area Scan Cameras Datasheet, Basler, https://graftek.biz/system/files/5686/original/Basler_Ace_Data_Sheet.pdf

[3] VMEbus International Trade Association, "American National Standard for VME64 Extensions" , ANSI/VITA 1.1-1997, Approved October 7, 1998, http://www.vita.com

[4] A20-2eSST Intel Core 2 Duo CPU Board 6U VMEbus Datasheet, MEN, https://www.men.de/products/discontinued-products/a20

[5] J-J. Savioz, "Beam Synchronous Timing Receiver Interface for the Beam Observation System", Engineering Specification, LHC project Document No. LHC-BOBR-ES-0001, 30-09-2003.

[6] R. Jones, "VME64x Digital Acquisition Board for the LHC Trajectory and Closed Orbit System" , Engineering Specification, LHC Project Document No. LHC-BP-ES-0002, 09-03-2004.

[7] M. Arruat *et al.*, "Front-End Software Architecture", in *Proc. ICALEPCS'07*, Knoxville, TN, USA, Oct. 2007, paper WOPA04, pp. 310-312.

[8] A. Dworak, F. Ehm, P. Charrue and W. Sliwinski, "The new CERN Controls Middleware", *Journal of Physics Conference Series*, vol. 396, Dec. 2012.

[9] Basler Pylon - Programmer's Guide and API Reference, Basler, http://mlab.no/blog/wp-content/uploads/2009/06/basler_pylon_prog_guide_and_api_ref.pdf, Feb. 2008.

[10] A25 - Embedded Single Board Computer with Intel Xeon D - 6U VMEBus for Industrial Applications - Datasheet, MEN, https://www.men.de/products/a25