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THE TIMING SYSTEM OF HIRFL-CSR

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Abstract

This article gives a brief description of the timing system for Heavy Ion Research Facility in Lanzhou-Cooler Storage Ring (HIRFL-CSR). It introduces in detail mainly of the timing system architecture, hardware and software. We use standard event system architecture. The system is mainly composed of the events generator (EVG), the events receiver (EVR) and the events fan-out module. The system is the standard three-layer structure. OPI layer realizes generated and monitoring for the events. The intermediate layer is the events transmission and fan out. Device control layer performs the interpretation of the events. We adopt our R&D EVG to generate the events of virtual accelerator. At the same time, we have used our own design events fan-out module and realize distributed on the events. In equipment control layer, we use EVR design based on FPGA to interpret the events of different equipment and achieve an orderly work. The timing system realizes the ion beam injection, acceleration and extraction.

INTRODUCTION

HIRFL-CSR (Heavy Ion Research Facility in Lanzhou-Cooler-Storage-Ring) is a multi-purpose CSR system that consists of a main ring (CSRm), an experimental ring (CSRe), and a radioactive beam line (RIBLL II) to connect the two rings. Figure 1 show an Overall Layout of HIRFL-CSR [1]. The two existing cyclotrons SFC (K = 69) and SSC (K = 450) of the HIRFL will be used as its injector system. The heavy ion beams with the energy range of 8–30 MeV/u from the HIRFL will be accumulated, cooled and accelerated to the high-energy range of 100–400 MeV/u in the main ring, and then extracted fast to produce RIB or highly charged heavy ions. The secondary beams (RIB or highly charged heavy ions) will be accepted and stored by the experimental ring for many internal-target experiments or high-precision spectroscopy with beam cooling. On the other hand, the beams with the energy range of 100–900 MeV/u will also be extracted from CSRm by using slow extraction or fast extraction for many external-target experiments.

CSR is a double ring system. In every operation cycle, the stable-nucleus beams from the injectors are accumulated, cooled and accelerated in the main ring (CSRm), then extracted fast to produce RIB or highly charged ions. The experimental ring (CSRe) can obtain the secondary beams once for every operation cycle. The accumulation duration of CSRm is about 10 s. considering the ramping rate of magnetic field in the dipole magnets to be 0.1–0.4 T/s, the acceleration time of CSRm will be nearly 3 s. Thus, the operation cycle is about 17 s [2].

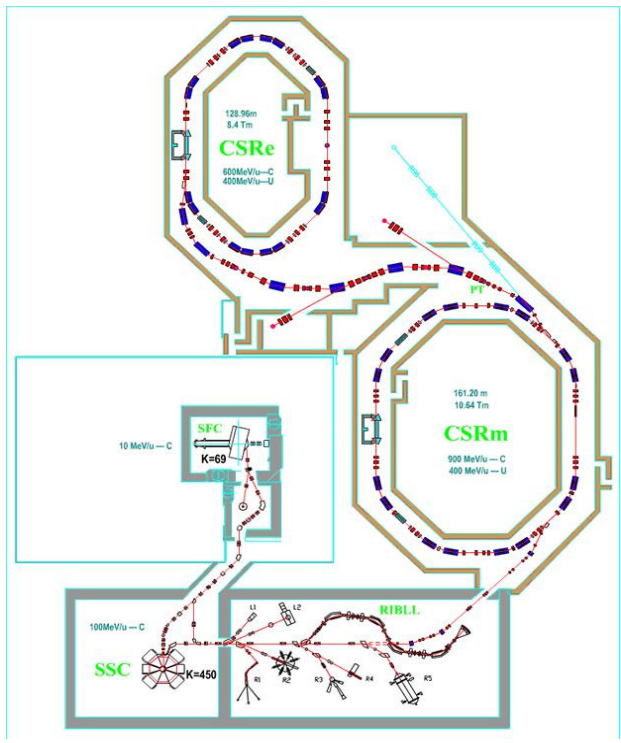

Figure 1: Overall Layout of HIRFL-CSR.

SYSTEM INTRODUCTION

The CSR is a synchrotron system, and the injection, acceleration, accumulation and derivation of the cluster must be precisely synchronized to achieve a successful operation cycle. CSRm infuses the CSRe with a beam once every other cycle, and CSRe can use the storage (or deceleration) of the beam to continuously target the target experiment. This precise synchronization is performed by the timing system and the magnetic field power control system. The time of the cluster in the CSR main ring is approximately 0.5us ~ 3us [3].

The timing system not only completes the normal control function, but more importantly the synchronization between the control equipment. For example, a successful independent cycle (from injection to derivation) of the CSR main ring requires a strict synchronization between CHOPPER, BUMPER, RF, QUADRUPLE, KICKER, and so on. The synchronization control function is the most complex and difficult key part of the control system. The success of the CSR control scheme lies in the ability to realize the synchronization of relevant equipment in the accelerator system and the most complicated and difficult key part of the system. Only by accurately pressing the accelerator requirement to achieve the synchronization function, the CSR can modulate the ideal beam with the expected target. Figure 2 shows the

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structure of the CSR synchronization control system. The synchronous control system connects all parts with Ethernet as the transmission medium: synchronous server, database, front-end server, front-end controller. The database system and synchronous server is the information and control centre of the whole system. The main function of the synchronization server is to organize the synchronization data of the CSR tuning bundles to all related devices, including the distribution of synchronous data and the generation and broadcast of timing. Synchronous data is a case table of the device's waveform data and device response. CSR database mainly adopts the ORACLE database system, main storage data structure information, the accelerator static attribute information, accelerator operation of real-time information, accelerator operation historical information, the accelerator malfunction of log information and so on five aspects. The synchronous database is one of the subsystems, which mainly stores the synchronous data of the equipment that is well organized. I/O controller and the DSP implementation parts perform specific operations role, they can finish and synchronous communication between the server and a controller is responsible for one to four control device object. The front-end server completes the collection of the output information of the controlled device object and the data exchange with the database system, and also provides the man-machine interface. Synchronous fan out is mainly used to distribute a synchronous instance in the timing sequence.

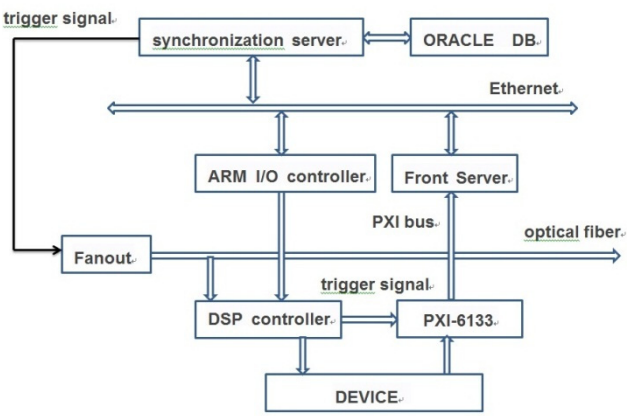

Figure 2: The structure of the CSR synchronization control system.

HARDWARE

HIRFL - CSR current way is composed of a piece of the story card (FPGA card PXI bus) based on virtual accelerator software is responsible for time series output to meet the requirements of optical signal pulse sequence (the smallest unit of pulse time is 20 nanoseconds), is converted to electrical signals through the light to electric switch, via the twisted-pair (150 meters) distributed to each control station control system. In each station control system is converted to light pulse signal through electrical signal to optical signal converter, and then fan out through light and the optical fiber distributed the light pulse signal to the control system of workstation front controller (DSP). In the front-end controller, it is interpreted and compared with the pre-deposited cases to determine whether the waveform output is carried out. The structure is shown in the Figure 3.

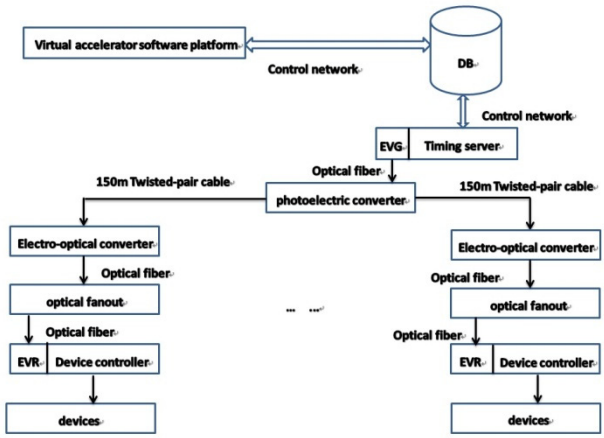

Figure 3: The structure of the hardware.

SOFTWARE DESIGN

There are three types of software for the timing system. The specific contents are as follows:

The CSR Cycle

The composition of the CSR cycle is as follows:

1） EVT_Start_Cycle
2） EVT_Prep_Inj
3） EVT_Inj_Start
4） EVT_Ramp_Start, EVT_Mid_Start
5） EVT_Prep_Ext
6） EVT_Ext_Start
7） EVT_End
8） EVT_MeasureN

The transmission and storage of a given data curve (node, cycle) within the DSP execution component needs to be triggered by an event to be implemented; some events have nothing to do with DSP. After decoding, it can trigger the self-process of certain devices, such as injection process, kicking the electromagnet power discharge, beam diagnosis...; many events are generated under certain conditions, such as the state of the equipment, external interruption, etc., such as the discharge event of the electromagnet power supply during the derivation, the beginning of one cycle, etc. Some events can change the course of the cycle or even interrupt the cycle.

The event can be divided into four categories according to the starting conditions. Sequence events: after the previous event, no special conditions can be started; External trigger timeout event: triggered by an external trigger. If timeout, start the scheduled timeout event; Trigger event outside: triggered by an external trigger. Even if timed out, the sequence of events continues; External trigger long wait event: the event starts with an external trigger or starts after the maximum wait time.

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The Event Table

Type description: Event code is a binary array and the length is 32 bits. The number of event ID in the table represents the total number of instances of an accelerated cycle. Event IDn indicates the number of instances to be executed in order of expedited order. Event ID delay time (unit is 20 ns) indicates how long the delay will be done after receiving the current case. The trigger output pulse width is a pulse signal that the EVR needs to output a case after the event is received, which is used to trigger the relevant device action, and the pulse width is determined by 40ns. The data file structure of the event table is shown in Figure 4. The event story structure is shown in Figure 5.

the number of event ID in the table
event ID1
Event ID delay time (unit is 20 ns)
event ID2
Event ID2 Delay time value
.....
Event IDn
Event IDn Delay time value
Trigger the output pulse width (unit is 40 ns)

Figure 4: The data file structure of the event table.

bits	31	30	29--25	24	23--16	15--8	7--0
value	1	1					
instruction	head of the code		reserve	mode	Event no.	Function code	virtual accelerator no.

Figure 5: The event story structure.

The GUI

For physical events the GUI (Graphical User Interface) is used to write the event sequence cycle to the RAM on the EVG, read the event sequence cycle from RAM and start the event cycle. Moreover, the GUI can exchange data with the Oracle database [4]. Figure 6 shows the event cycle sequence organizing GUI.

Figure 6: The event cycle sequence organizing GUI.

The event cycle story structure is shown in Figure7.The number of events means the number of events in the sequence of the CSR cycle. Length of the string means length of the whole sequence data string. Event IDn indicates the number of instances to be executed in order of expedited order. Delay time means delay time before to start next event, unit is μs. Repeat times means how many repeat times when Generator output the event ID.

the number of events
length of the string
event ID
delay time
repeat times

Figure 7: The event cycle story structure.

SUMMARY

The timing system has been applied to the actual operation in 2008 and passed the acceptance of the CSR expert group. It implements the requirements of the synchronization for the CSR project. The timing system has been stable operation of the nine-and-a-half years, and ensures the normal conduct of the experiment.

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